Modeling of HKMG Stack Process Impact on Gate Leakage, SILC and PBTI

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Purpose

- Gate stack process impact on gate leakage, SILC and PBTI is analyzed.
- IL and HK thickness and energy-barrier offsets' impact on gate leakage and SILC is quantified.
- Reaction-Diffusion-Drift (RDD) framework is used to simulate time kinetics of bulk traps for SILC, and IL/HK interface traps for PBTI.

Outline

- Introduction
- Experimental Details
- Gate Leakage Framework
- SILC Framework
- Peak SILC Response
- SILC Modeling of HKMG stacks
- RDD Model for Bulk Trap Time Kinetics
- RD Model for PBTI generated Trap Time Kinetics
- Conclusions

Introduction: Gate Leakage

- **Equivalent Oxide Thickness (EOT) scaling of High-K Metal Gate (HKMG) gate insulator is desirable.**
- **The primary impediment is gate leakage (I_{G0}) due to direct tunneling via the interlayer (IL) and High-K (HK).**
- **Due to less sensitivity to leakage, IL scaling is the preferred route to EOT scaling.**
- **However, the tunneling barriers between the Si/IL and IL/HK can also change for ultra-thin layers.**

Introduction: Stress Induced Leakage Current (SILC)

- **SILC related increase in gate leakage for HKMG NMOS gets exacerbated with EOT scaling.**
- **SILC is due to Trap Assisted Tunneling (TAT) via traps generated in the IL and HK.**
- **The exact location of generated traps for maximum SILC response is debated.**
- **The time kinetics of SILC shows power law time dependence with n ~ 1/3 for HKMG stacks.**

Introduction: Positive Bias Temperature Instability (PBTI)

- **PBTI in NMOS and NBTI in PMOS related increase in threshold voltage shift (ΔV_T) gets worse with EOT scaling.**
- **PBTI is due to trap generation at the IL/HK interface (ΔN_{IT-HK}) and inside the HK bulk (ΔN_{OT-HK}) and electron trapping in the HK bulk (negligible).**
- **The ΔN_{IT-HK} dominates overall ΔV_T for PBTI stress.**
- **Measured time kinetics of ΔN_{IT-HK} show power law time dependence with n ~ 1/6 time slope.**

Device Details

- **Measurements are done on Gate First HKMG NMOSFET devices**
- **Chem-Ox IL devices were processed by using RT wet chemistry followed by standard 8 hour air-break prior to ALD HfOx deposition.**
- **Low T RTP is used for the formation of ultra-thin IL down to 3 Å.**
- **Post HK nitridation (PHKN) has been done using Decoupled Plasma Nitridation (DPN) followed by Post Nitridation Anneal (PNA).**
- **SILC during PBTI stress in measure-stress-measure (MSM) mode. PBTI trap generation at the IL/HK interface is studied using Direct Current IV (DCIV) method in MSM mode.**

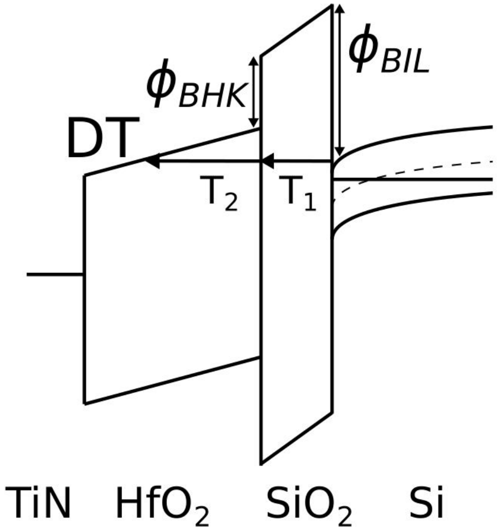
Device Details

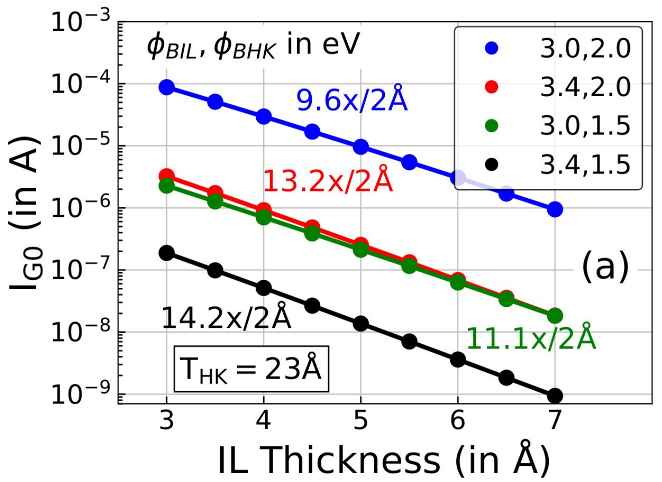
Device	Pre-IL	IL	Pre-HK	HK	Nitridation	SILC	DCIV
D1	Type-A	Chem-Ox 6.5Å	Type-I	18Å	No	✓	
D2	Type-A	Chem-Ox 6.5Å	Type-I	23Å	Yes	✓	
D3	Type-A	RTP-5Å	Type-IV	23Å	No	✓	✓
D4	Type-B	RTP-3Å	Type-IV	23Å	No	✓	✓
D5	Type-B	RTP-3Å	Type-III	23Å	No	✓	✓
D6	Type-C	RTP-3Å	Type-II	18Å	No	✓	
D7	Type-C	RTP-3Å	Type-II	23Å	No		✓
D8	Type-C	RTP-3Å	Type-IV	23Å	Yes		✓

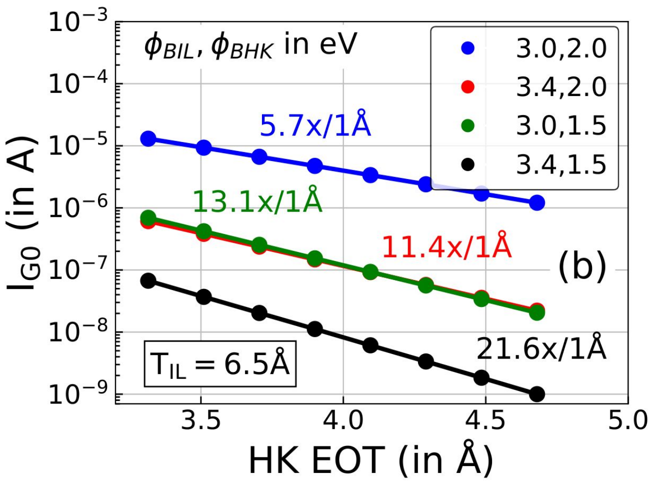
Gate Leakage Framework

WKB tunneling probabilities via IL (T_1) and HK (T_2) and supply function in cathode govern gate leakage (I_{G0})

$$I_{G0} \propto \int S_n(f_c - f_a)T\,dE$$





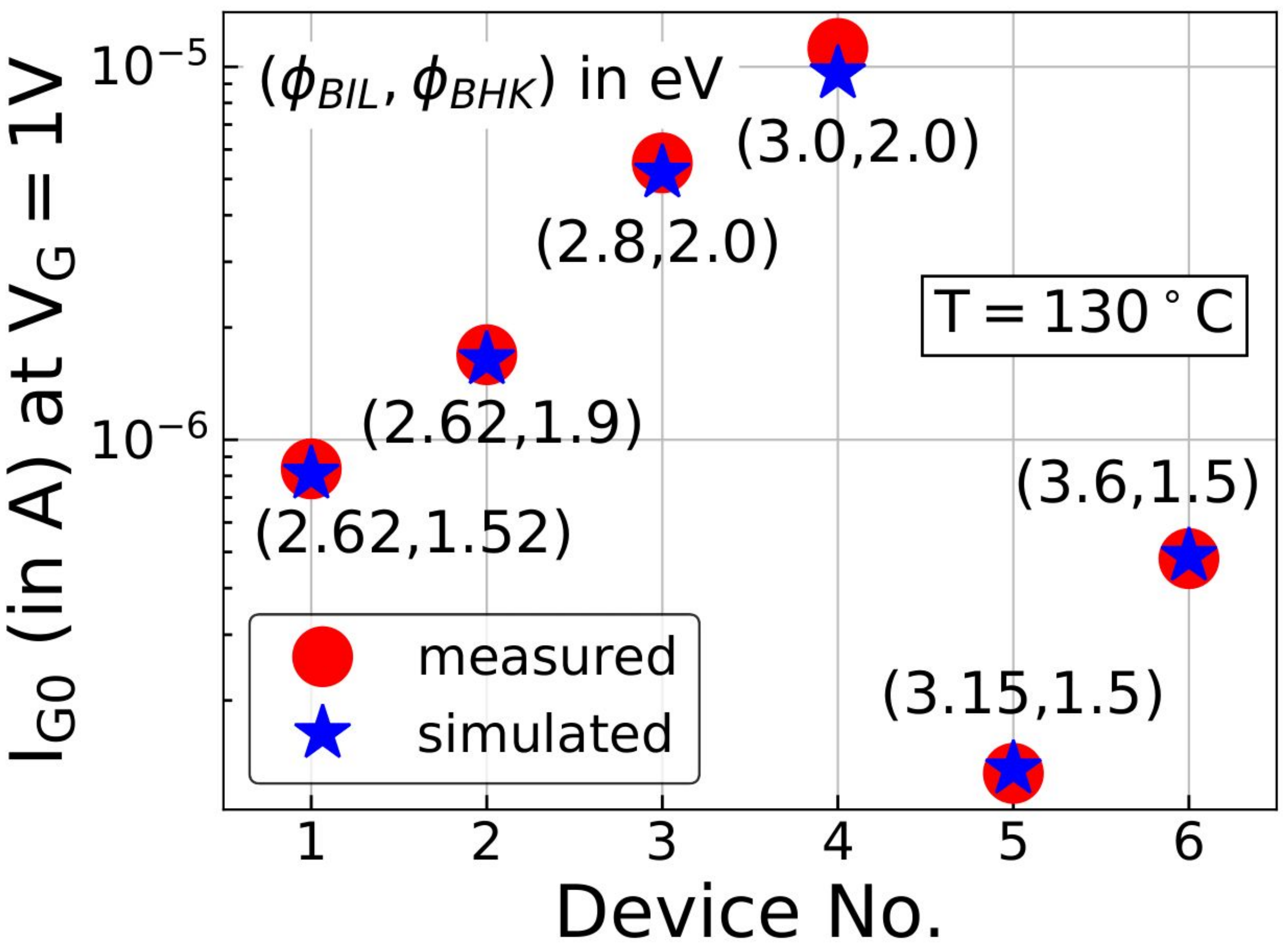


Typical rate of I_{G0} increase for scaling IL (10X/2Å) and HK (10X/1Å EOT) becomes different when φ_{BIL} and φ_{BHK} changes are also considered.

Gate Leakage Framework

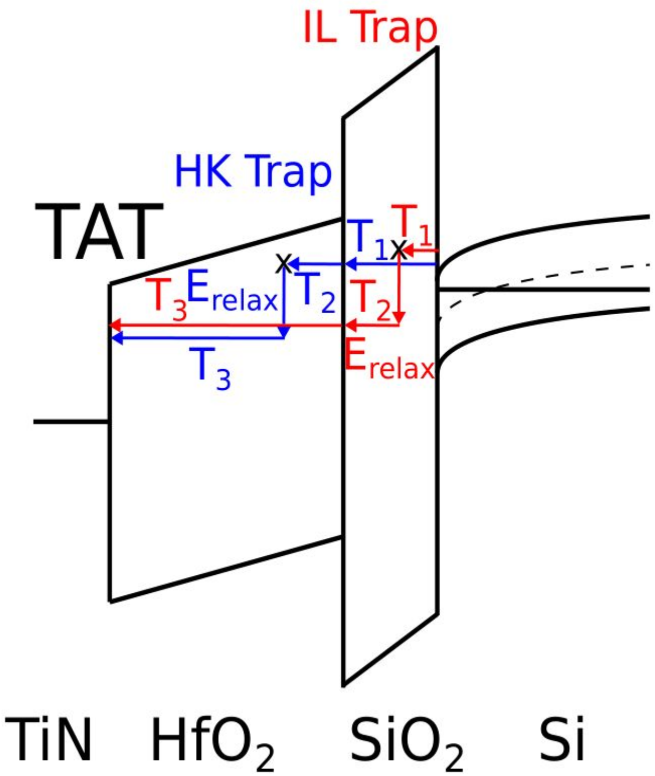
- **The measured and modeled gate leakage across devices is shown.**

- **The same energy barriers are used to model SILC.**



SILC Framework

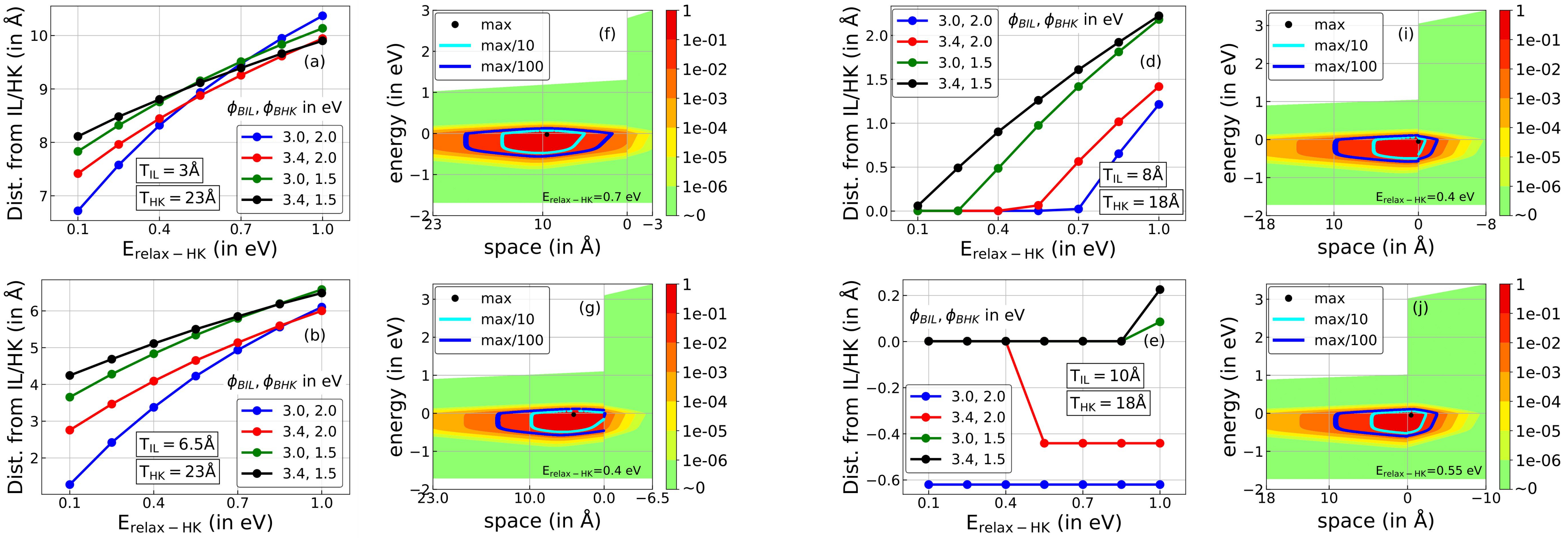
- **SILC is due to TAT via traps generated at IL and HK bulk during PBTI/TDDB stress.**
- **Based on trap location (in IL or HK), the probabilities T_1, T_2 and T_3 are calculated.**
- **Energy relaxation in the IL is taken as 1 eV.**

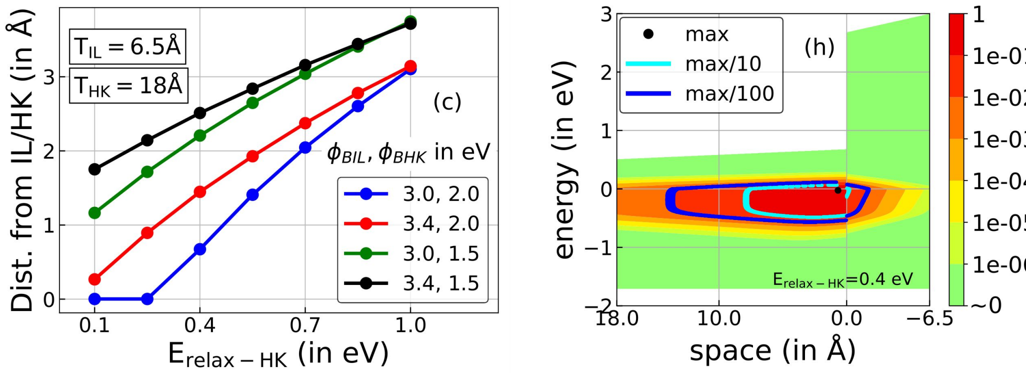


$$\Delta I_G = \iint c\, \Delta N_{OT}(x,t) \frac{T_{c,t}(E)T_{t,a}(E-E_{relax})}{T_{c,t}(E)+T_{t,a}(E-E_{relax})} dx\, dE$$

$$c = q\sigma_n v_{th} N_C S_n (f_c - f_a)$$

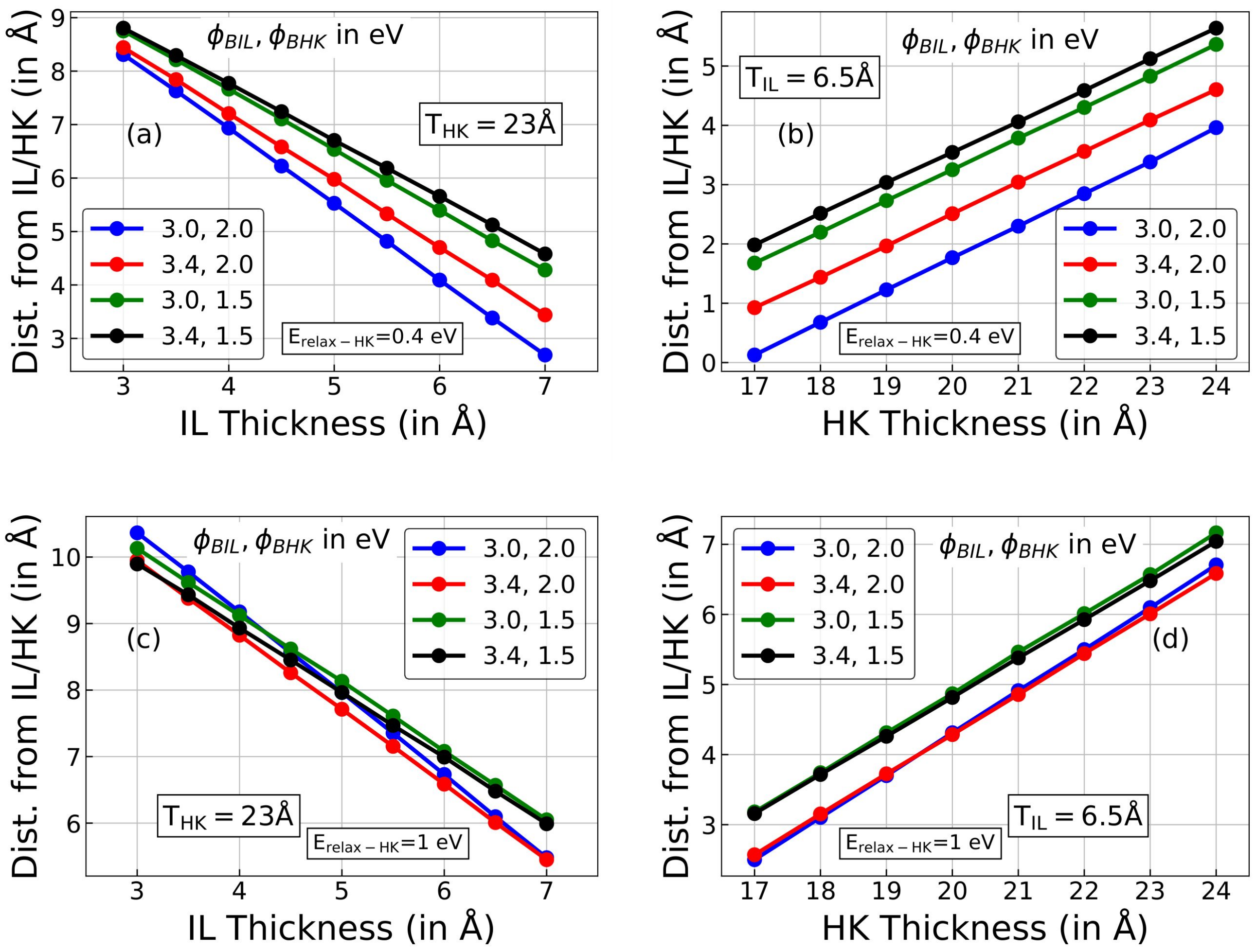
Peak SILC Response





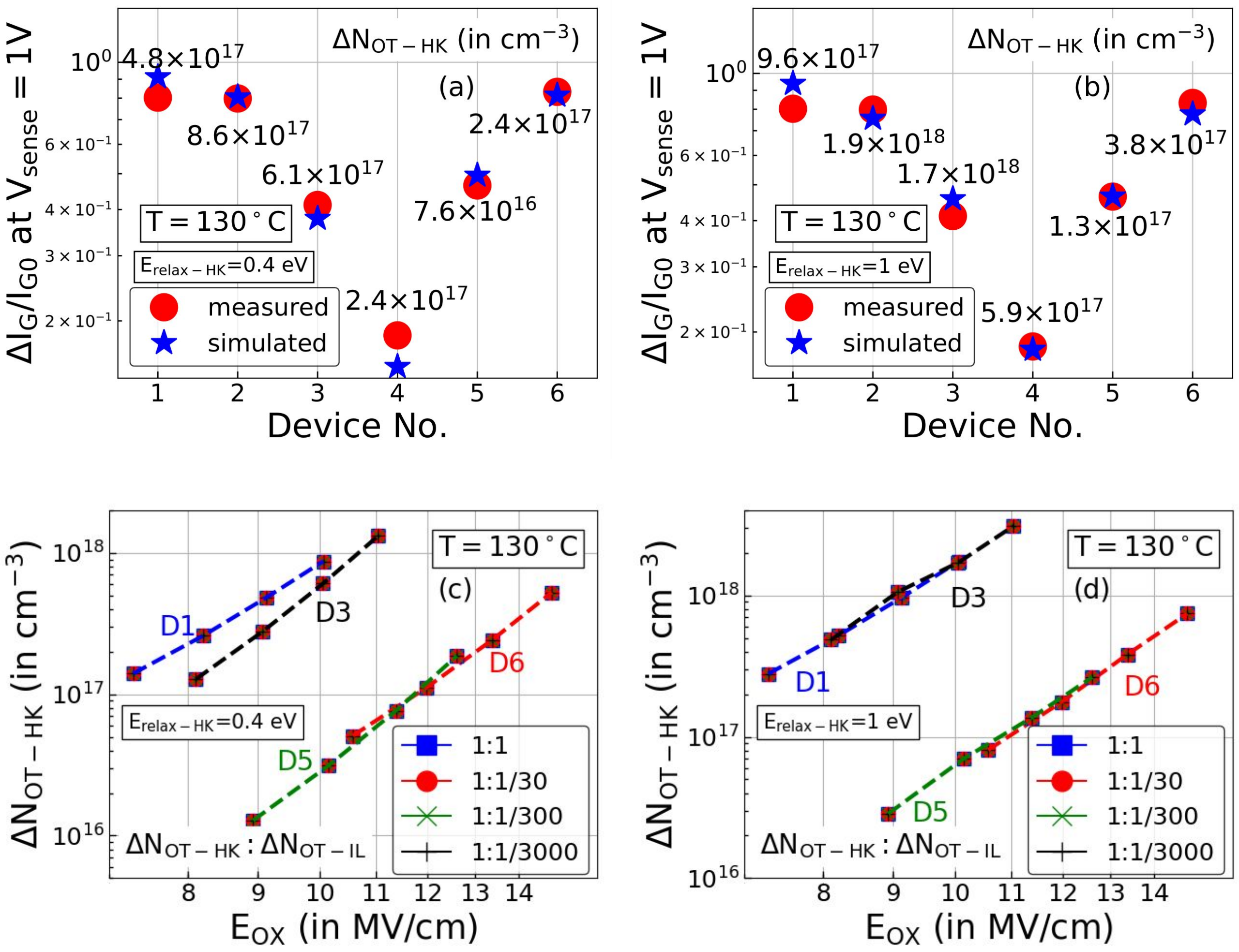
The maximum response point and the contours move from HK to IL as the ratio IL thickness/HK thickness is increased.

Peak SILC Response



- **The maximum response point moves deeper into HK for lower IL thickness.**
- **The maximum response point moves towards IL/HK interface for lower HK thickness, more so for higher φ_{BHK}.**

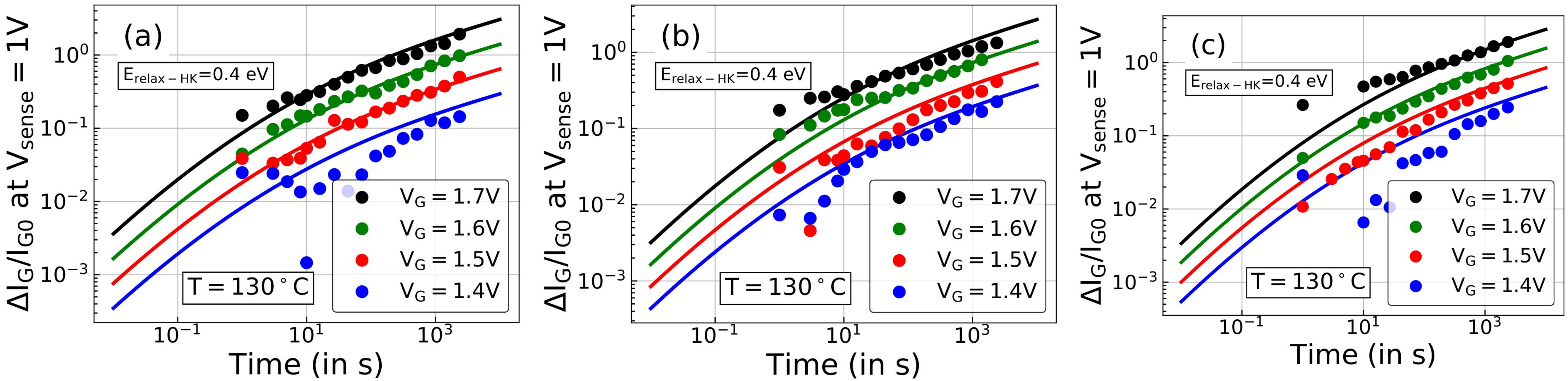
SILC Modeling of HKMG Stacks



- **HK bulk trap density values (ΔN_{OT-HK}) decrease as the HK relaxation energy is decreased.**

- **SILC is dependent mainly on ΔN_{OT-HK} and insensitive to changes in bulk trap density in IL (ΔN_{OT-IL}), across different E_{OX}.**

SILC Modeling of HKMG Stacks: Time Kinetics



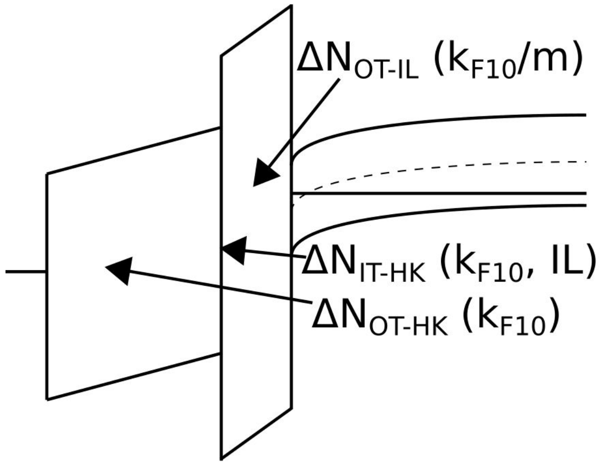
Measured and delay-corrected data and modeled SILC time kinetics and modeling for (a) D6, (b) D2, (c) D1.

Device	IL (in Å)	HK (in Å)
(a) D6	3	18
(b) D2	6.5	23
(c) D1	6.5	18

RDD Model for Bulk Trap Time Kinetics

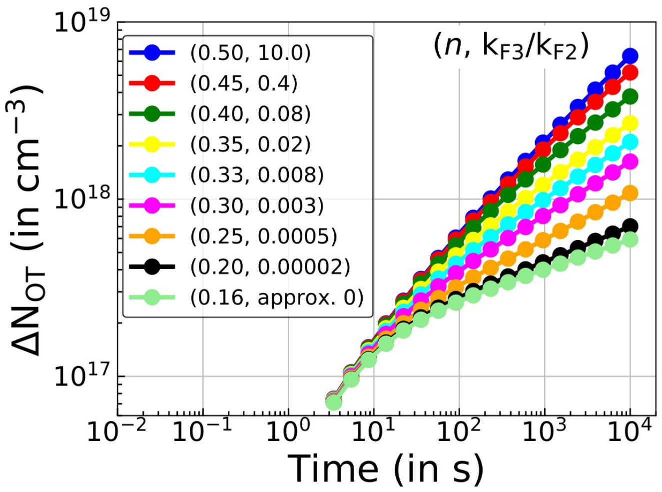
- **RDD Chemical Equations:**

$$X\text{-}H + HE\ (k_{F1}, k_{R1}) = X^{-} + H \quad (1)$$
$$Y\text{-}H + H\ (k_{F2}, k_{R2}) = Y^{-} + H_2 \quad (2)$$
$$Z\text{-}O + H + HE\ (k_{F3}, k_{R3}) = Z^{-} + OH^{-} \quad (3)$$
$$k_{F1}=k_{F10}*\exp((\Gamma_0+\alpha/kT)E_{OX})*\exp(-E_{AkF1}/kT)$$

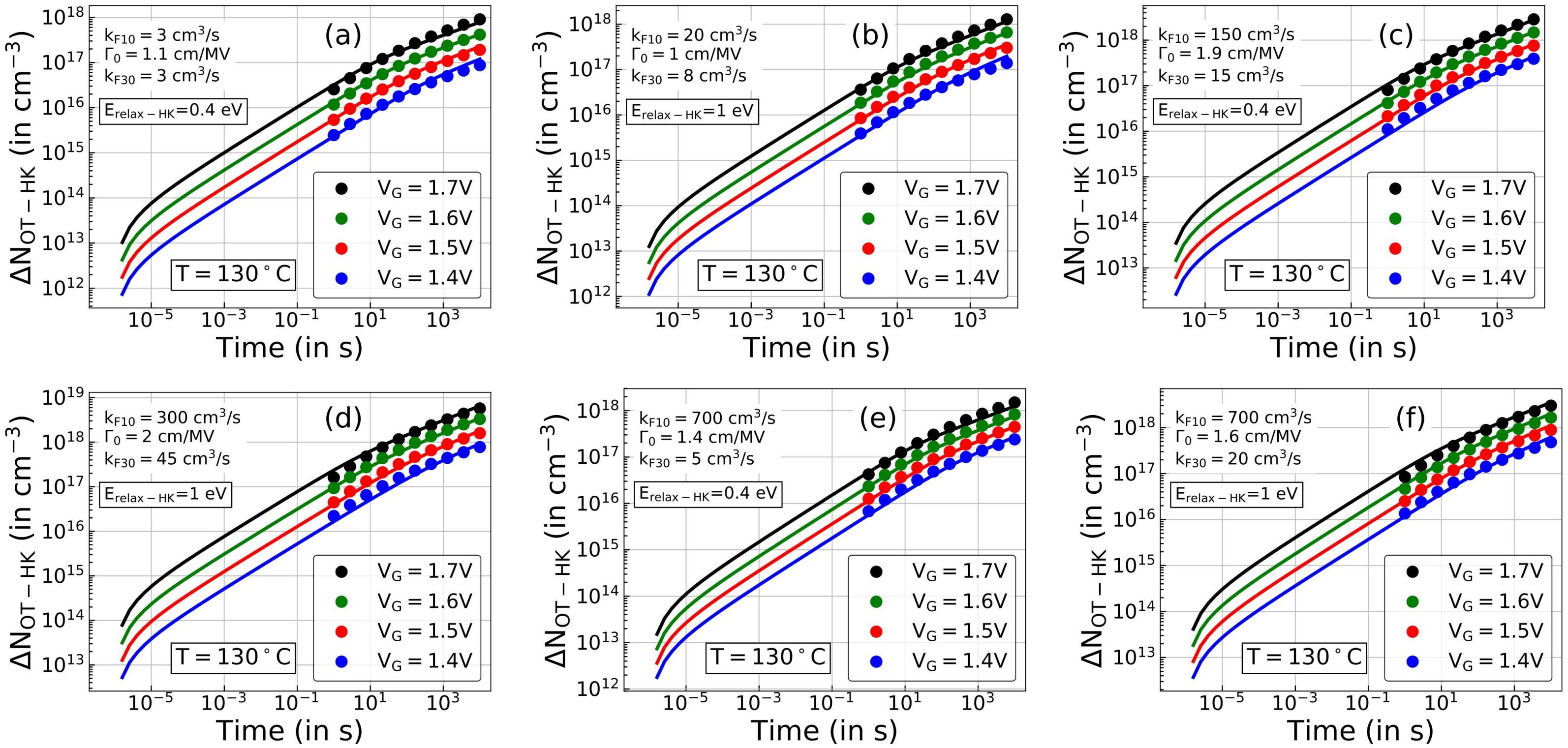


- **Release of H, H induced bond dissociation and eventual diffusion and drift of molecular (H_2) and ionic (OH^-) species control ΔN_{OT} time kinetics.**

- **Simulated stress time kinetics of ΔN_{OT} for different k_{F3} shows the slope variation.**



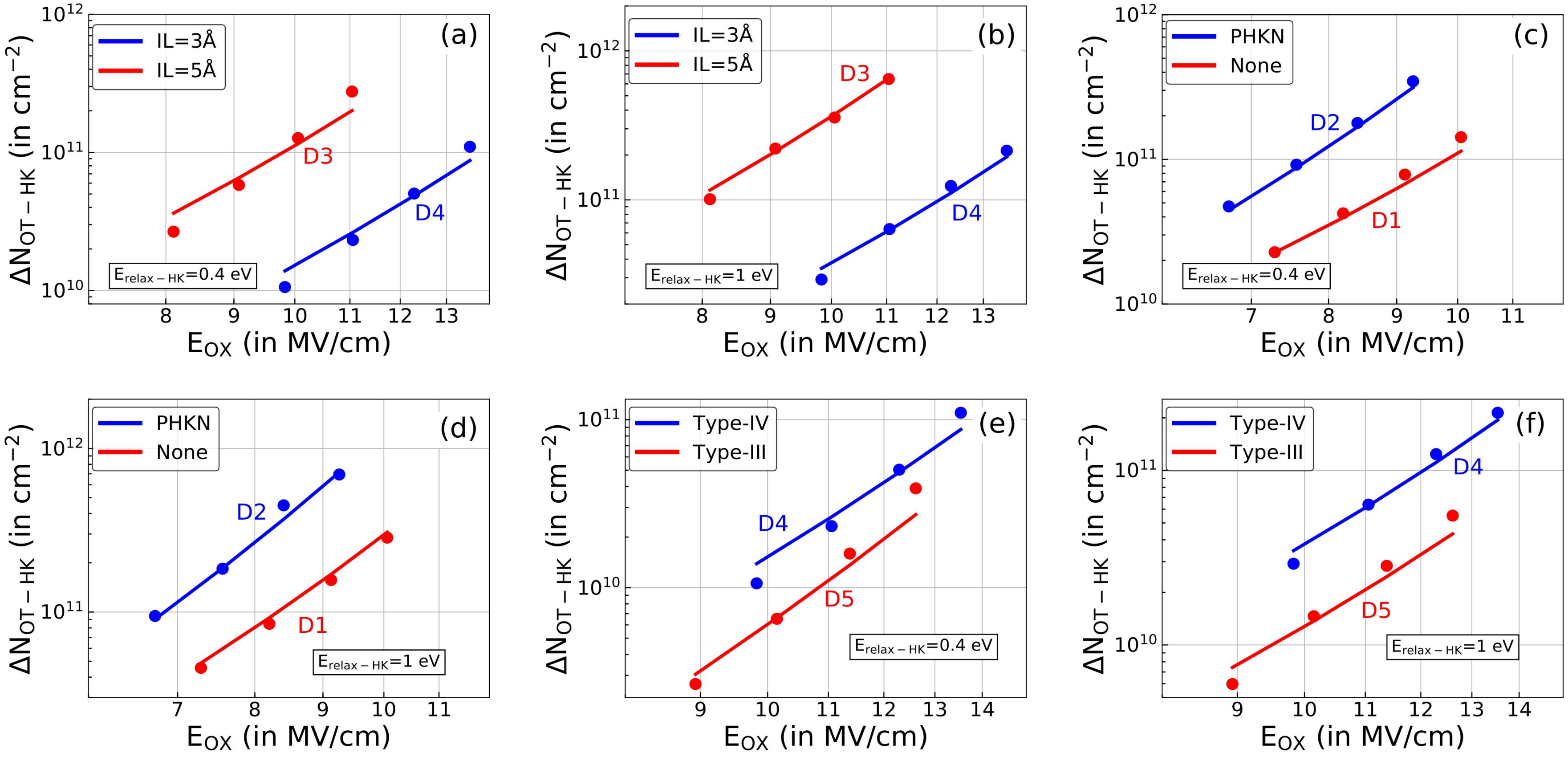
RDD Model for Bulk Trap Time Kinetics



ΔN_{OT-HK} (trap generation rate ratio IL:HK= 1:300) time kinetics and RDD modeling for (a)-(b) D6, (c)-(d) D2, (e)-(f) D1.

Parameters	Value Used
k_{F20}	5.75×10^3 cm^3/s
k_{R10}	5×10^4 cm^3/s
k_{R20}	7.5×10^{-4} cm^3/s
k_{R30}	7.5×10^{-4} cm^3/s
α	0.5 qÅ
E_{AkF1}	0.3 eV
E_{AkF2}	0.235 eV
E_{AkF3}	0.235 eV
E_{AkR1}	0.12 eV
E_{AkR2}	0.2 eV
E_{AkR3}	0.2 eV

Bulk Trap Generation: Process Impact



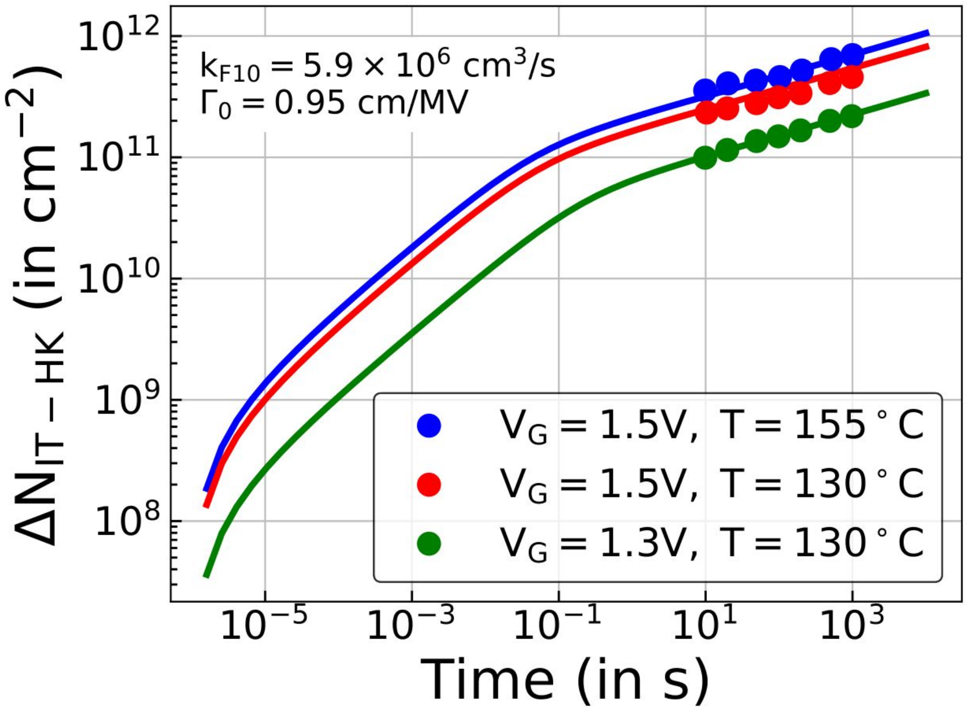
ΔN_{OT-HK} reduces as IL thickness is reduced, increases with PHKN and increases with higher moisture content (controlled by pre-HK IFT).

RD Model for PBTI generated Trap Time Kinetics

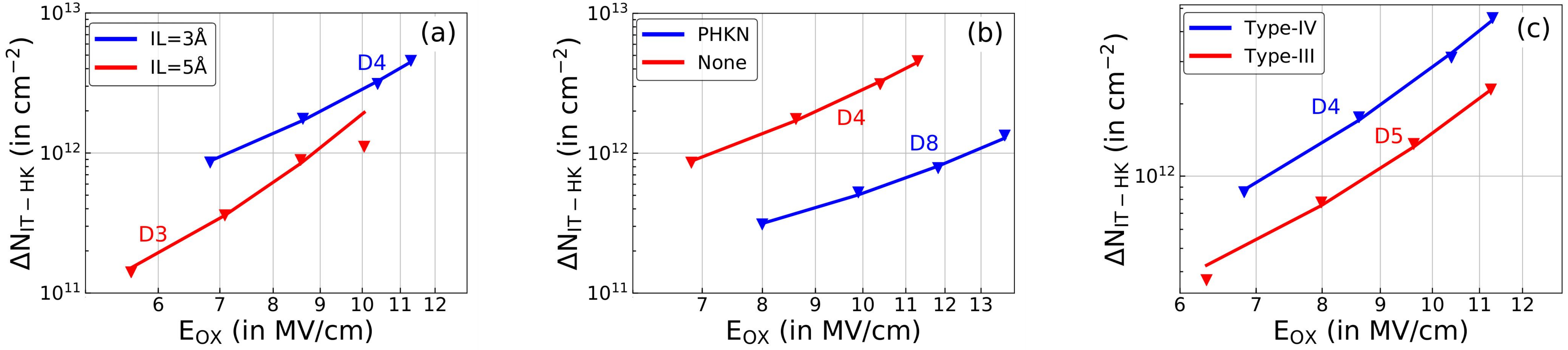
E_{AkF1} (RD)	0.2 eV

ΔN_{IT-HK} time kinetics is modeled using pure (H_2) diffusion.

Modeling of ΔN_{IT-HK} time kinetics at different V_G and across all devices is done using only 2 adjustable model parameters, k_{F10} and Γ_0.



PBTI generated Traps: Process Impact



- **E_{OX} dependence of ΔN_{IT-HK} and modeling for variation in (a) IL thickness, (b) PHKN, and (c) Pre-HK IFT is shown.**

- **With IL reduction ΔN_{IT-HK} increases, with PHKN it reduces and with IFT, it increases with higher moisture content.**

Conclusions

- **The composition and quality of the IL and HK integration processes impact leakage and reliability of ultra-thin HKMG stacks.**
- **Changes in energy barrier offsets should be considered for proper estimation of leakage increase at reduced IL and HK thickness.**
- **The dominating contribution to SILC is due to ΔN_{OT-HK} changes.**
- **The generic RDD framework (RD being a subset) is able to model the time kinetics of ΔN_{OT-HK} (ΔN_{OT-IL}) and ΔN_{IT-HK} and explain their power-law time slope at long time.**
- **The process dependence of ΔN_{OT-HK} and ΔN_{IT-HK} is modeled.**

Thank You!