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Estimation of Time to Failure Distribution in SRAM due to Trapped Oxide Charges

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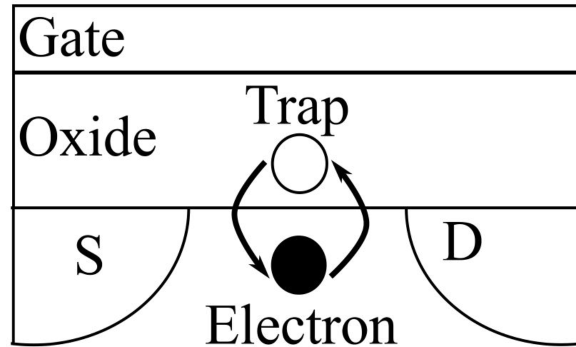
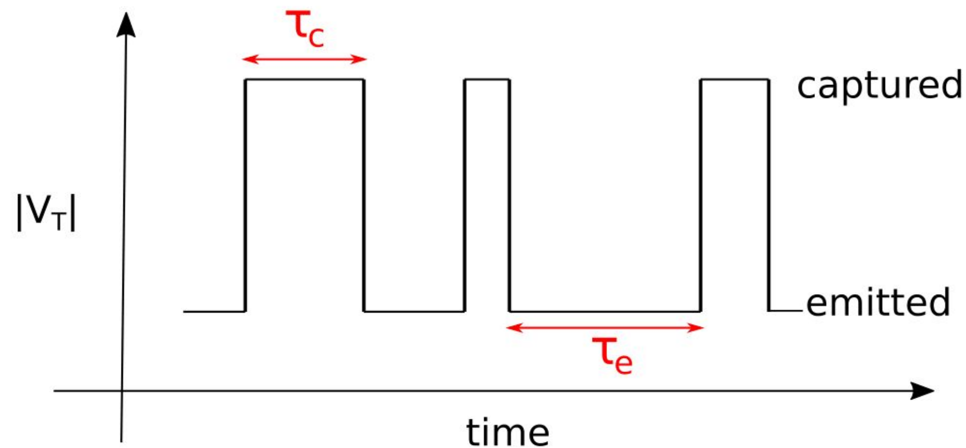
Random Telegraphic Noise (RTN)



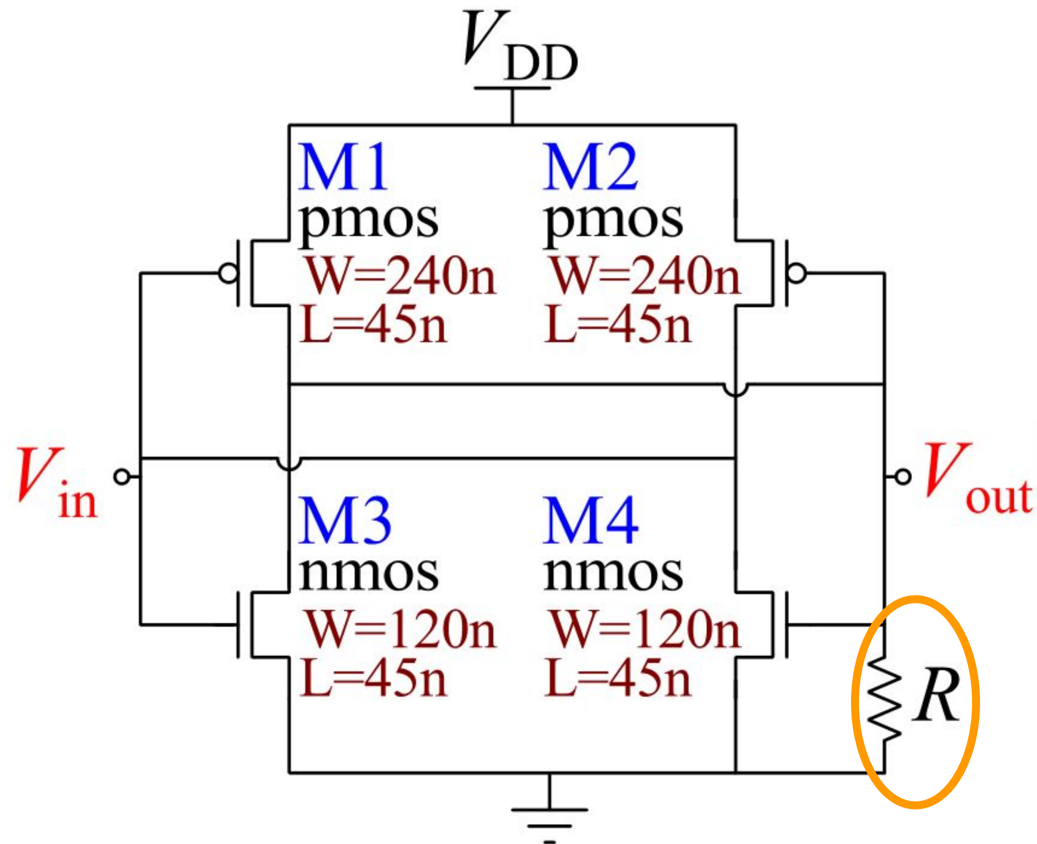
$$f(\tau_c) = \frac{1}{\bar{\tau}_c} e^{-\frac{\tau_c}{\bar{\tau}_c}}, \quad \tau_c \geq 0$$

$$f(\tau_e) = \frac{1}{\bar{\tau}_e} e^{-\frac{\tau_e}{\bar{\tau}_e}}, \quad \tau_e \geq 0$$



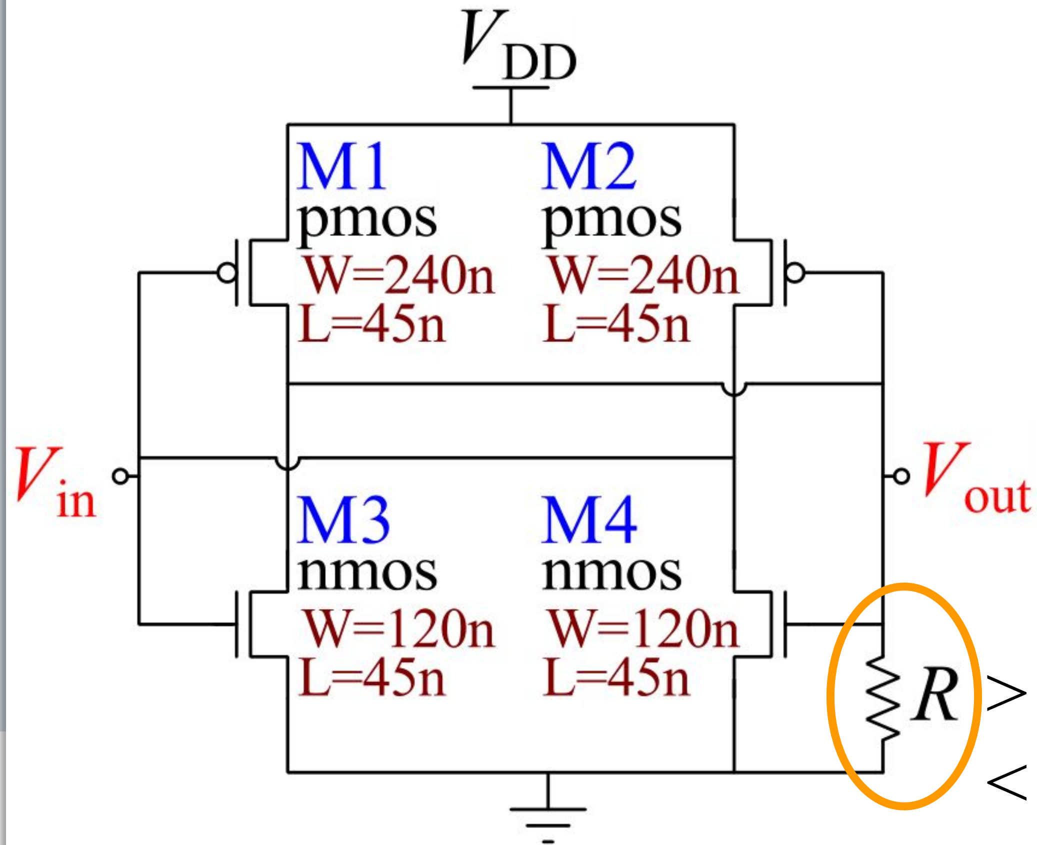
- **Trap captures an electron for time: τ_c**
  Trap has no captured electron for time: τ_e
- **τ_c and τ_e are random variables.**
- **The capture and release is modeled by two Poisson processes, which occur alternately one after each other.**

RTN Model in Circuit



- **The single trap RTN phenomenon is modelled using a resistor**
- **The time that the resistor is a part of the circuit: captured electron in trap The time for which the resistor is removed: released electron from trap**
- **Both these times are modelled as Poisson processes**

RTN Model in Circuit



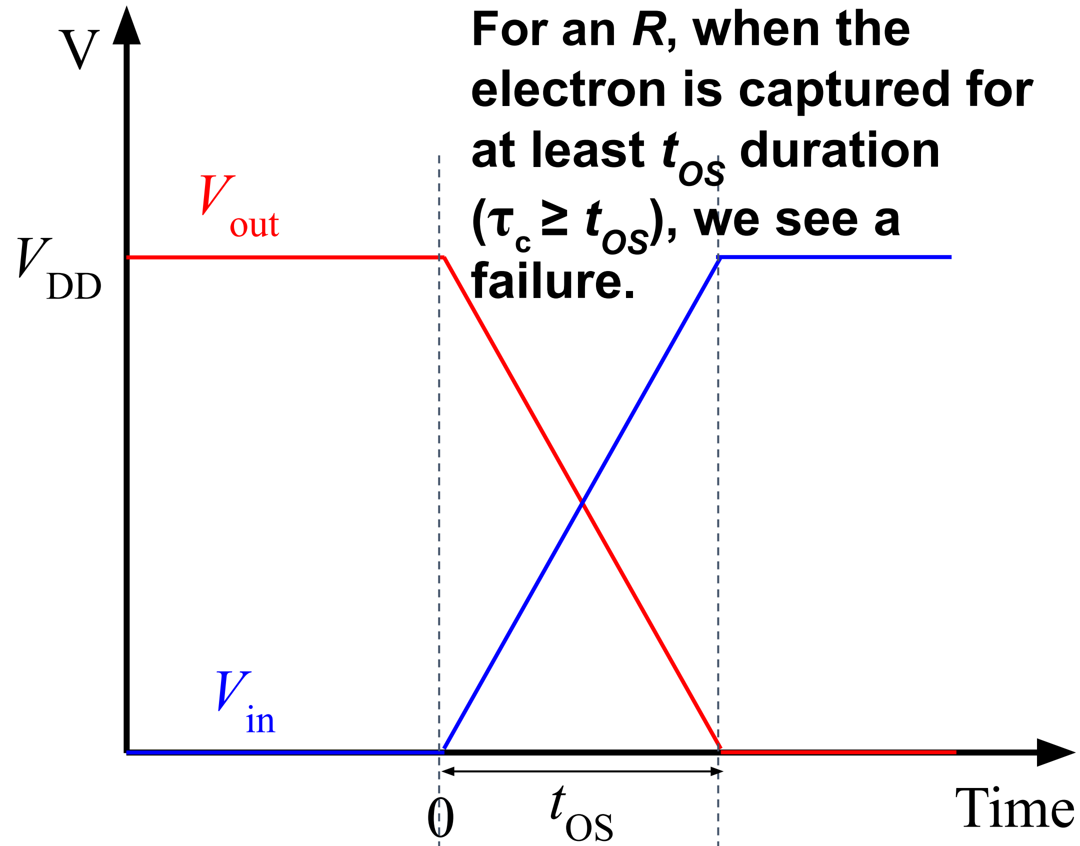
- **Resistance models leakage**
- **Above a certain *R*, the gate leakage is low enough that no failure occurs even if *R* is left in the circuit indefinitely**

$> R_{TH}$: No failure

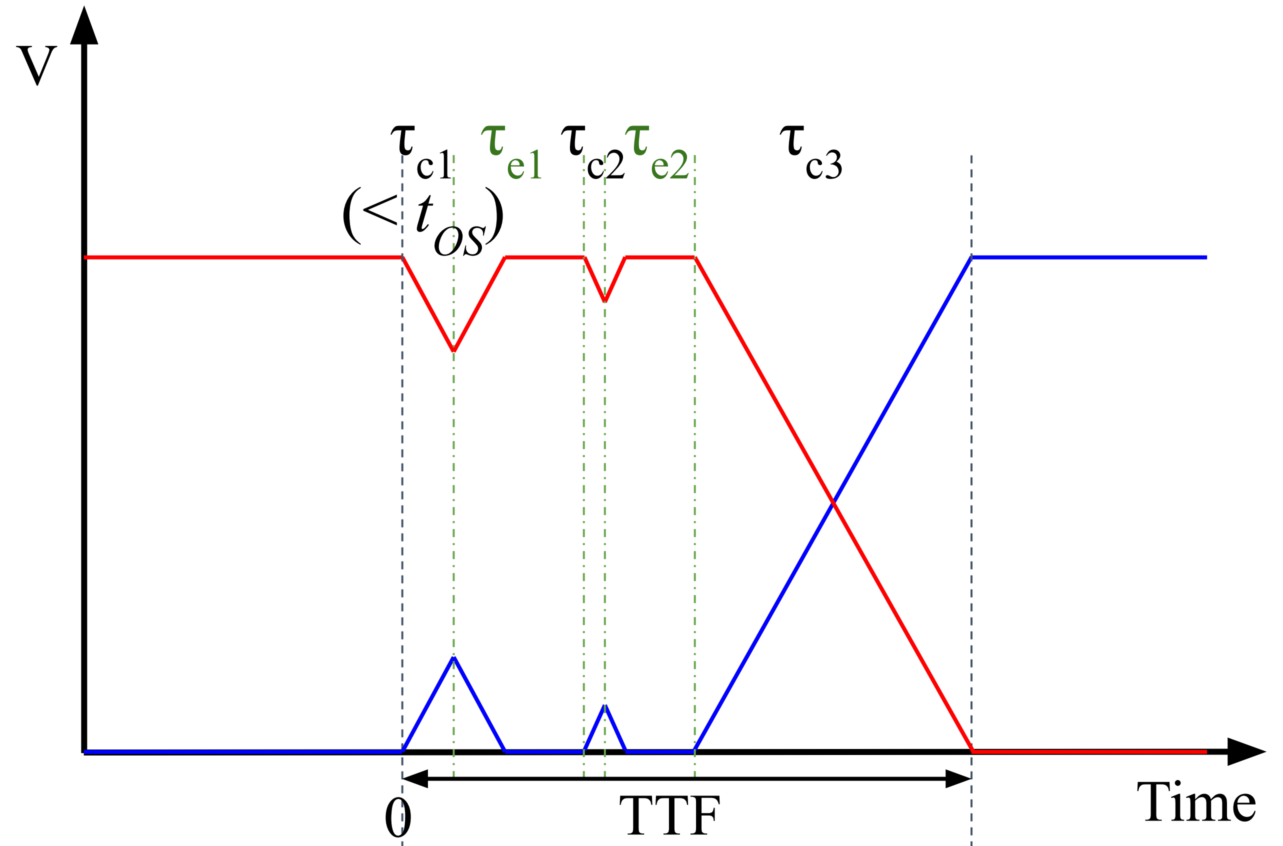
$< R_{TH}$: Failure time varies with R

We vary this *R*

Failure due to RTN



For an *R*, when the electron is captured for at least t_{os} duration ($\tau_c \geq t_{os}$), we see a failure.



***R* is never removed from circuit.**

***R* appears in circuit for τ_c time and is removed for τ_e time, till failure occurs**

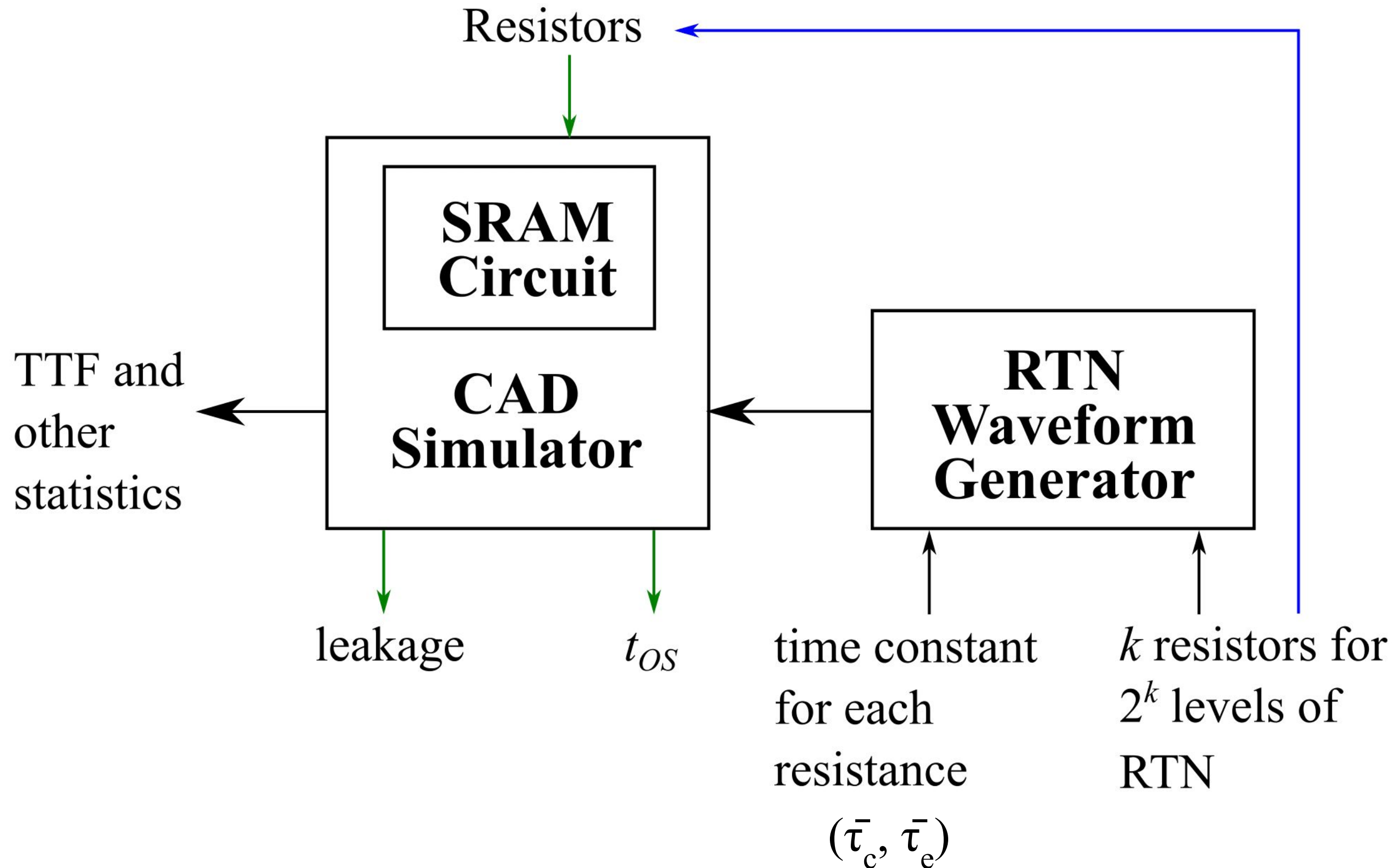
Simulation Methodology

$$f(\tau_c) = \frac{1}{\bar{\tau_c}} e^{-\frac{\tau_c}{\bar{\tau_c}}}, \quad \tau_c \geq 0$$

$$f(\tau_e) = \frac{1}{\bar{\tau_e}} e^{-\frac{\tau_e}{\bar{\tau_e}}}, \quad \tau_e \geq 0$$

- $\bar{\tau}_c = \bar{\tau}_e = \bar{\tau}$ **(for analytical convenience)**
- **Let T be the time to failure of a stored bit.**
  If $\bar{\tau} = 100t_{OS}$, Prob(T = t_{OS}) ≈ 0.99.
  So, $\bar{\tau}$ is selected in the range of $0.1t_{OS}$ to $10t_{OS}$.
- **Repeated Monte-Carlo trials (stochastic simulations) are run**

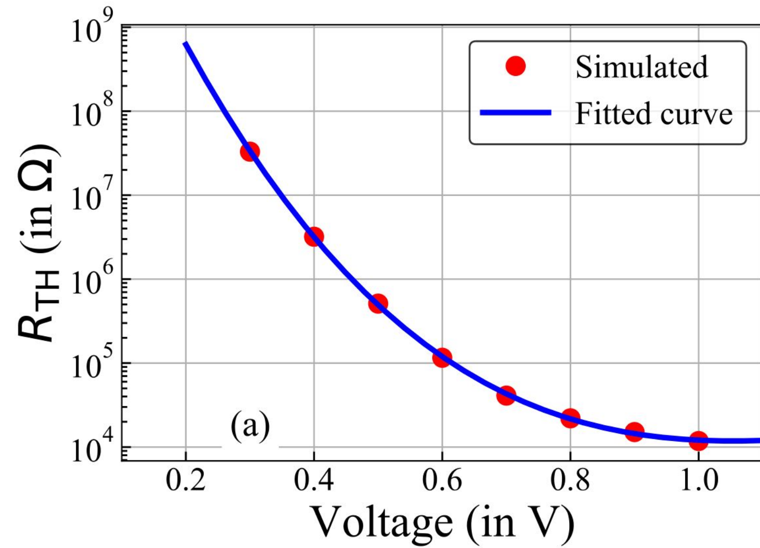
Overview: Method to Estimate TTF Distribution

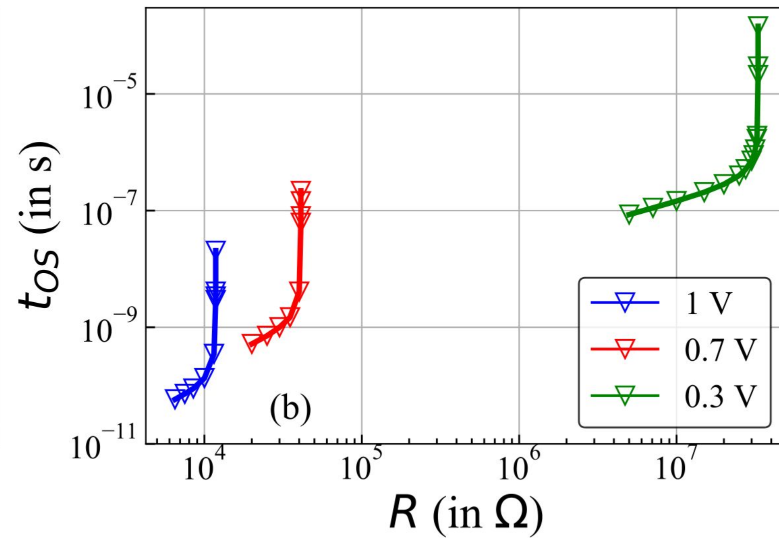


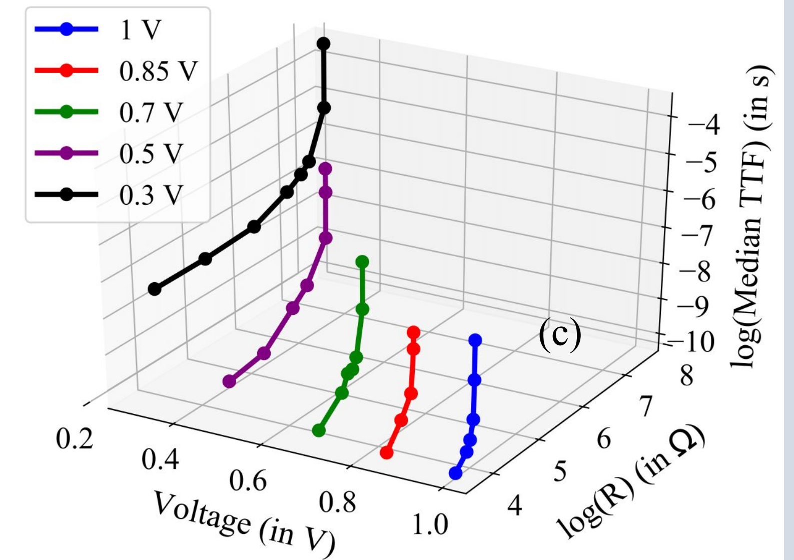
- **It is a combination of:**
  - **circuit level model of RTN**
  - **Monte-Carlo simulations**

- **This approach is flexible:**
  any circuit-level (or device level) model for RTN + Monte-Carlo methods
  = estimate the TTF distribution for any SRAM circuit.

Results





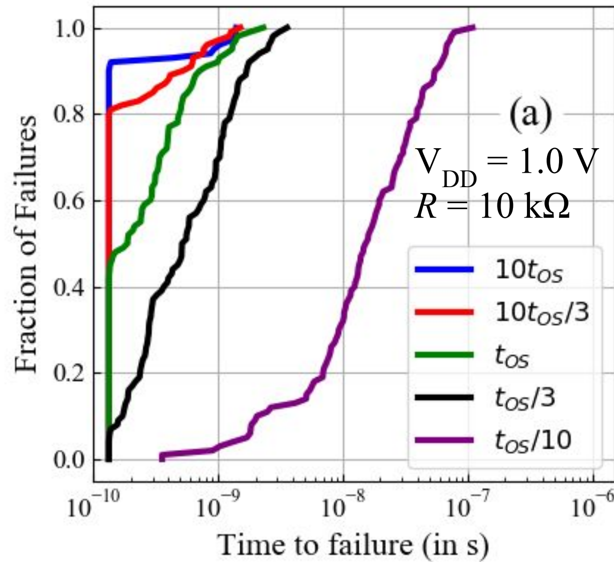


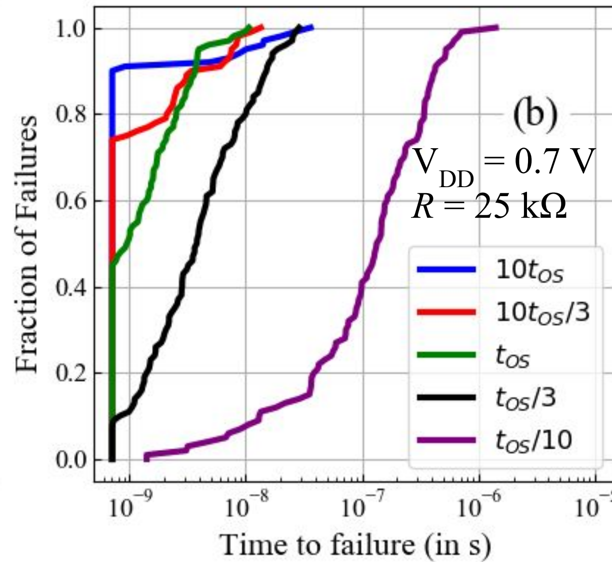
a) V_{DD} vs R_{TH}. For a V_{DD}, leakage below a certain value → no failure due to RTN.

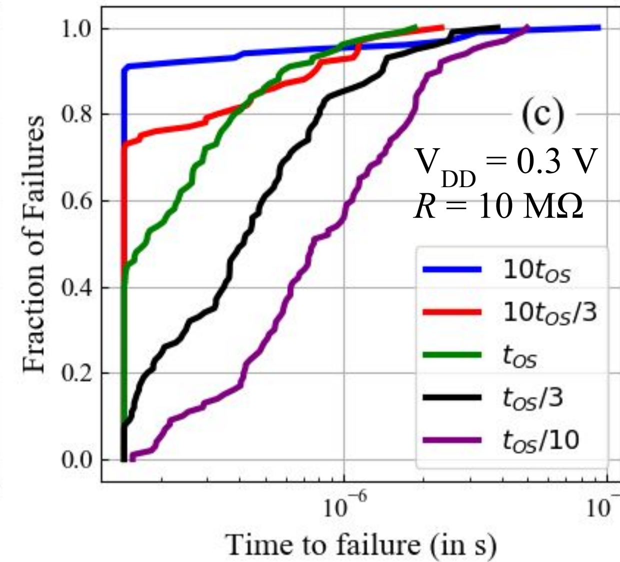
b) t_{OS} for different voltages has a singularity at R_{TH}.

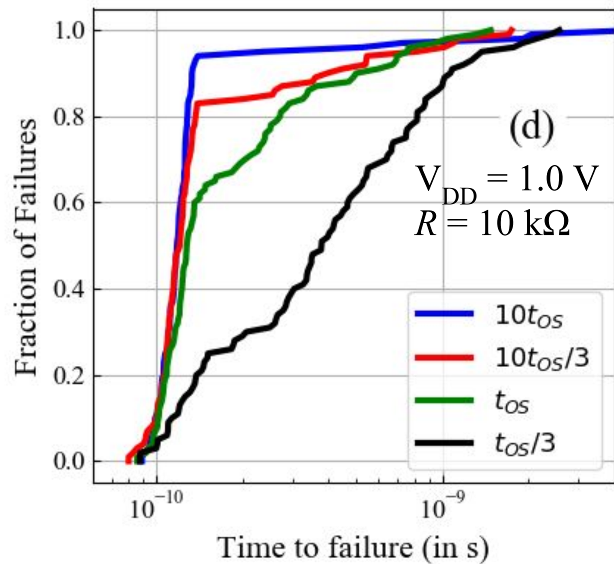
c) Median time to failure increases as we increase resistance or supply voltage, keeping the other fixed.

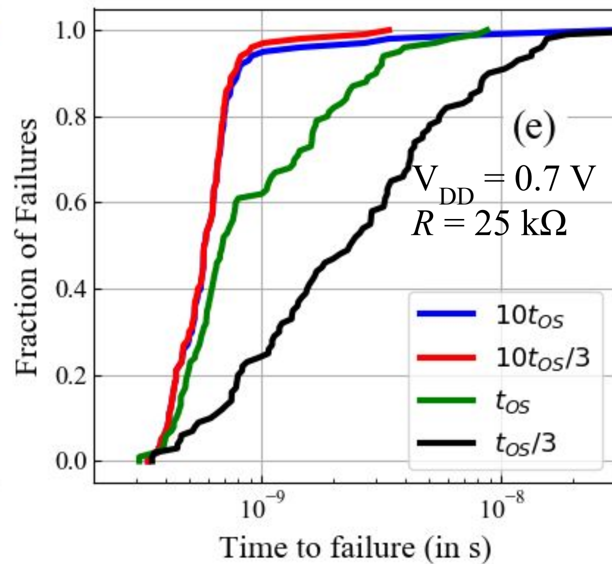
Results

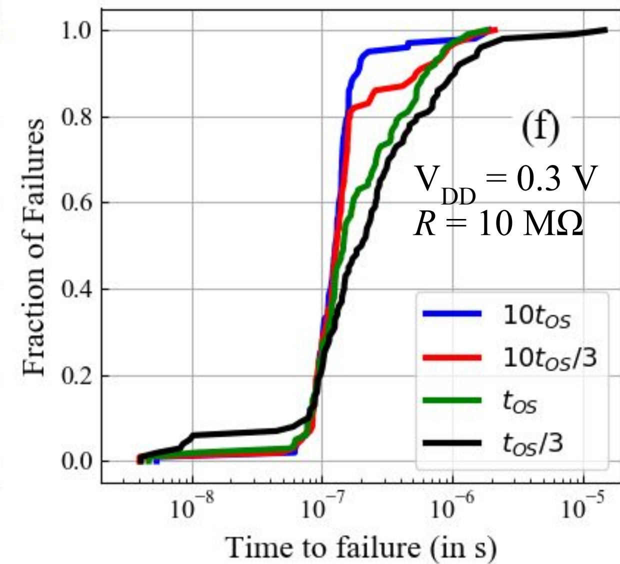












As we decrease the mean period of RTN, the distribution spreads across a higher range in time as compared to RTN with lower mean period.

Process Variations: The overall distribution worsens.

Summary

- Trapping and detrapping of charges in the oxide interface of a MOSFET leads to a random telegraphic noise (RTN) injection
- This event negatively affects the reliability of stored bit in an SRAM cell
- In this work, a method to estimate the statistical distribution of time to failure of a stored bit in an SRAM cell is proposed.
- The proposed method includes a composition of a trapping/detrapping current injection model, a Monte-Carlo simulator, and a circuit-level abstraction of an SRAM cell.
- As an example of the proposed method, using circuit-level simulations, the effect of RTN due to a single-trap model is showcased for 45 nm CMOS technology. Process variation simulations are also performed.