EE 611: Microwave Integrated Circuits
Butler Matrix Circuit: Project Report

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1 Aim of the Project

The Butler matrix is the most commonly used beamforming network that, in conventional form, is capable of producing M beams, where M is any integral power of 2. The butler matrix uses passive hybrid power dividers and fixed phase shifters to produce the desired progressive phase shifts at the elements of an antenna array necessary to form simultaneous multiple beams. Our aim is to design a broadband 4X4 Butler Matrix circuit using microstrip transmission line at the frequency of operation 5.4 GHz. The design is to be fabricated on FR4 substrate with $\epsilon_r = 4.4$, h = 1.6 mm, tan $\delta = 0.02$.

2 Simulation of Results using Ideal Elements

We used ADS software to design the Butler Matrix using ideal T-Lines. Since Butler Matrix is a combination of 90° hybrids and phase delay lines, we first designed a 90° hybrid. Then, taking the proper combination of 90° hybrids and delay lines, designed the 4X4 Butler Matrix.

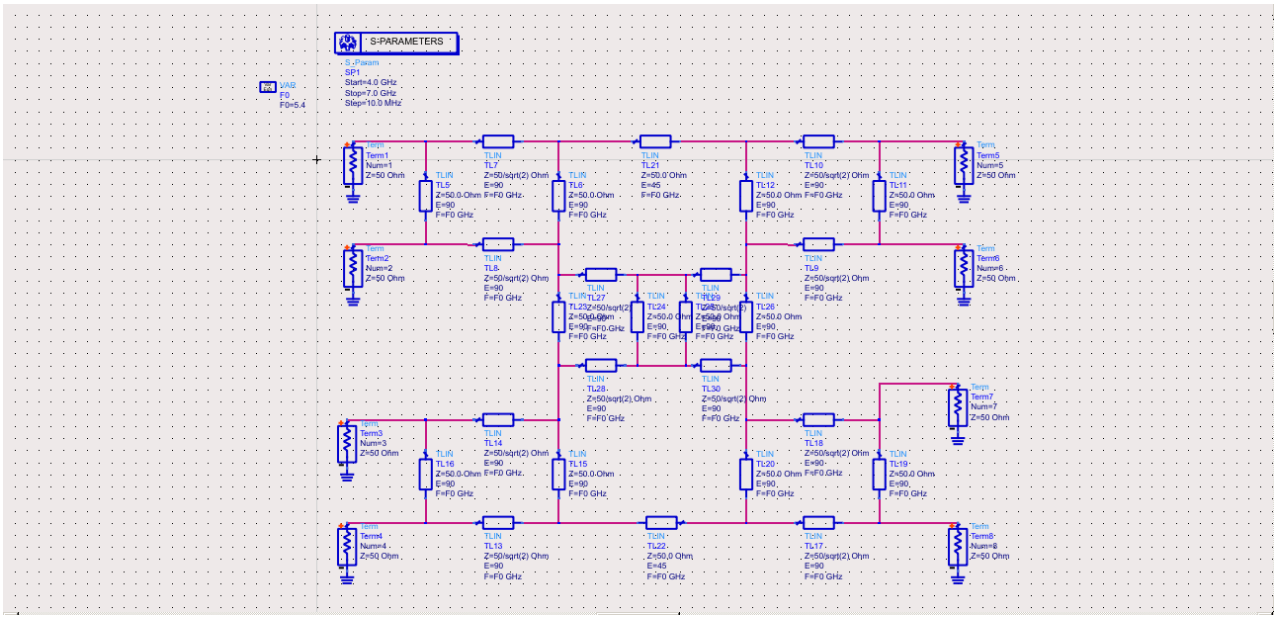


Figure 1: Schematic using Ideal Elements

Below, are the various simulation results:

2.1 Magnitude and Phase of s parameters between different Input and Output Ports

Using these plots, we can see phase relations between the various input and output ports are as expected and the power is divided equally between input and output ports. The phase shift between each beam should be $\phi = \frac{(2k-1)\pi}{n}$. For a 4x4 butler matrix we should get phase shifts of 45^o and 135^o.

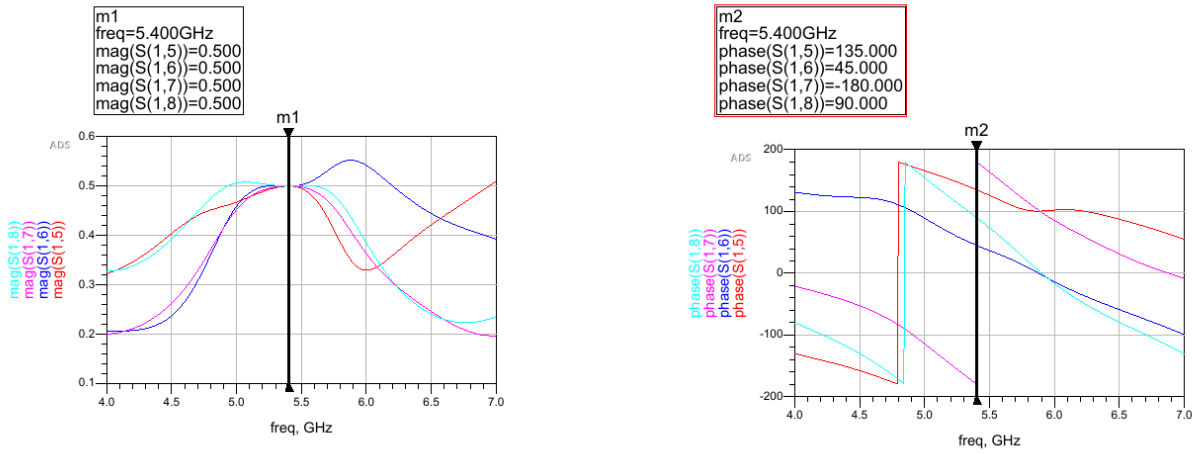


Figure 2: Input port 1

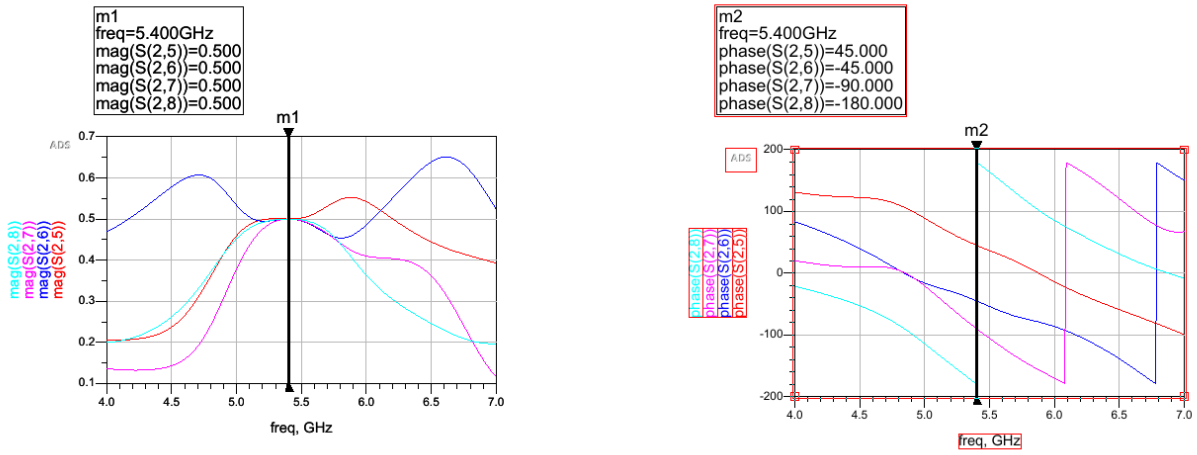


Figure 3: Input port 2

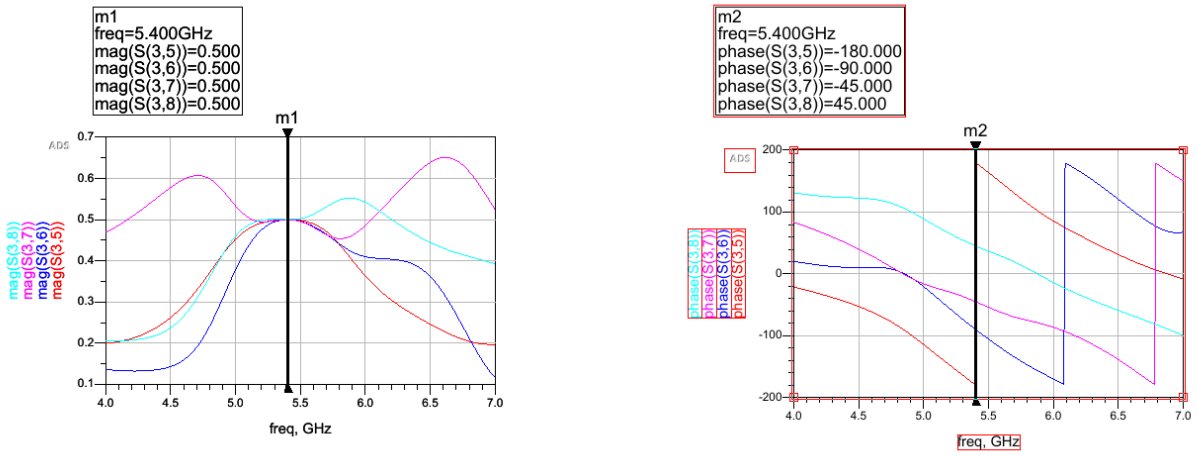


Figure 4: Input port 3

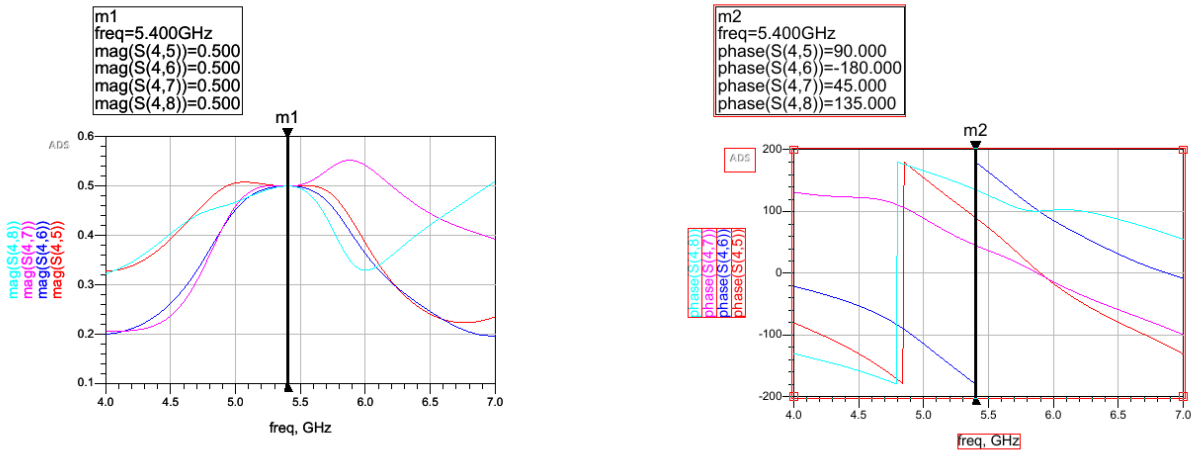


Figure 5: Input port 4

Since this is circuit is made using ideal T lines, we get perfect power division of 0.5 from every input to every output port. Also, the phase relations obtained between port 5 and port 7, port 6 and port 7 and port 6 and port 8 are multiples of $\frac{\pi}{4}$.

2.2 Magnitude and Phase of s parameters between Input ports

Using these plots, we can see that the input ports are isolated from each other.

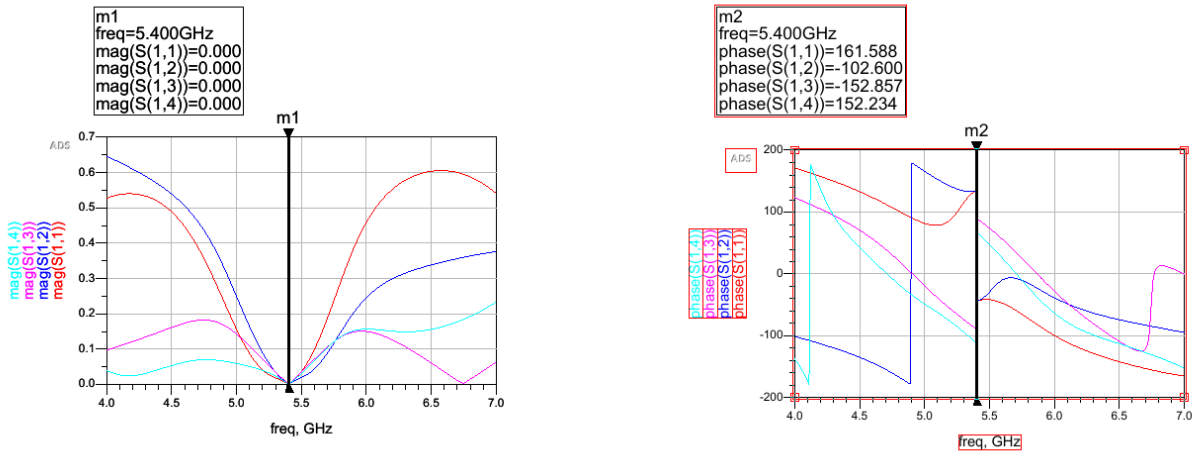


Figure 6: Input port 1

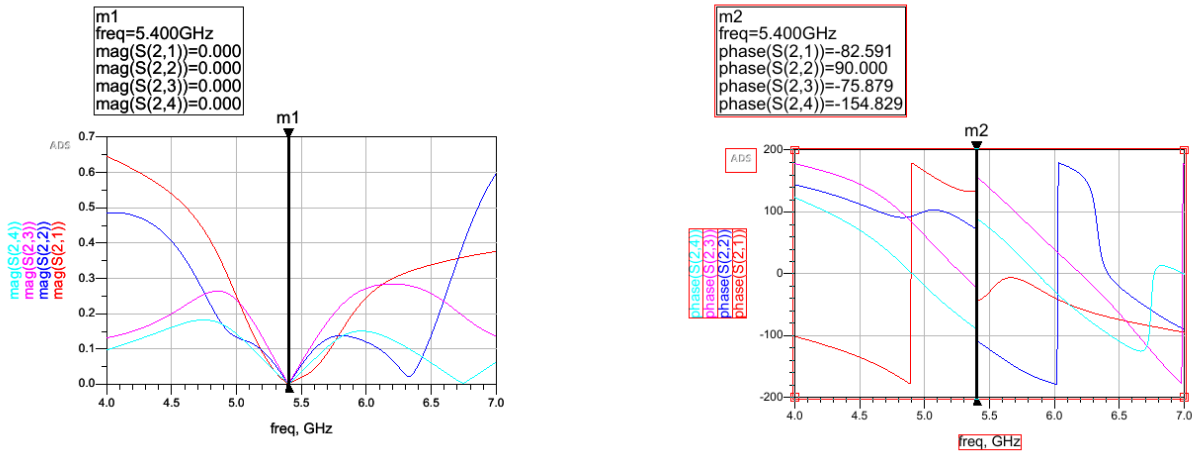


Figure 7: Input port 2

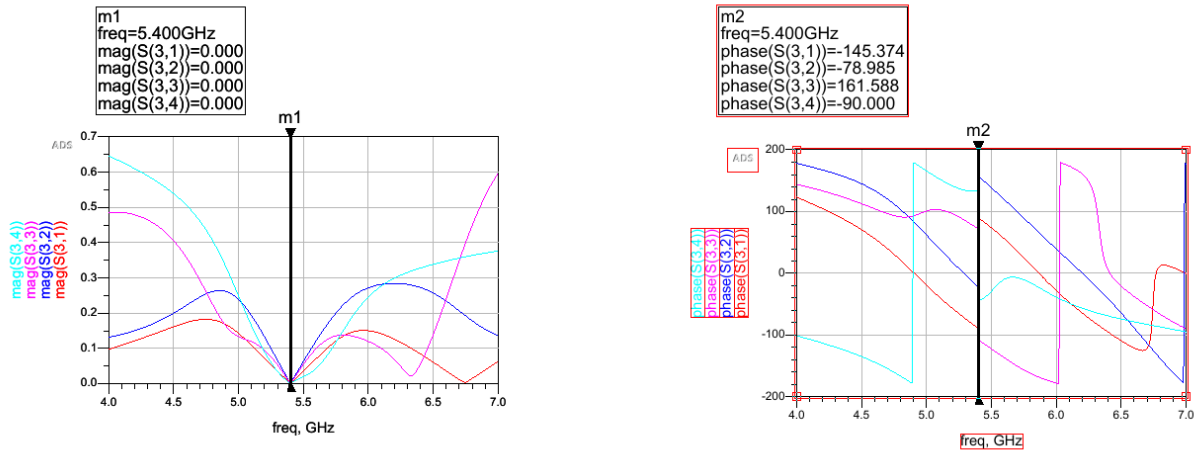


Figure 8: Input port 3

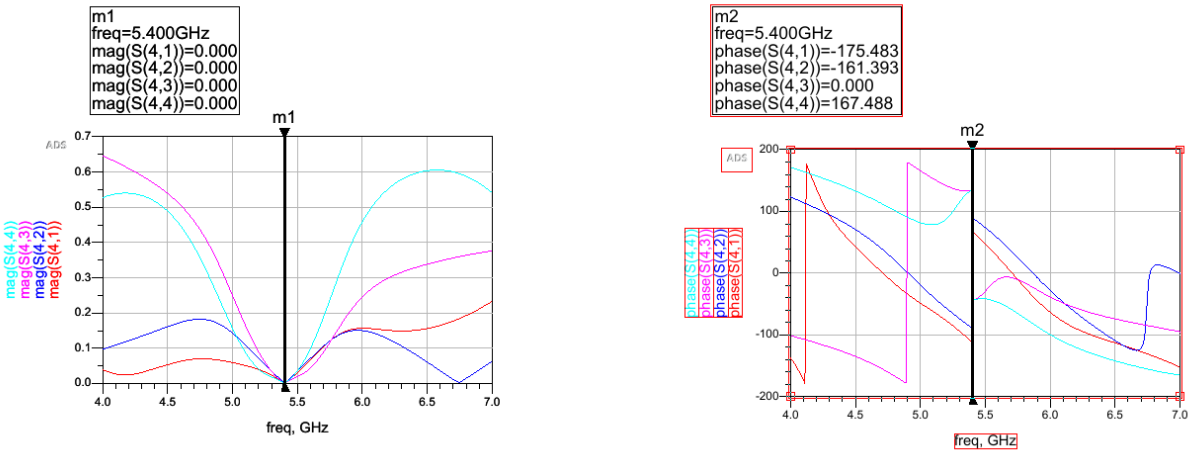


Figure 9: Input port 4

Since this is circuit is made using ideal T lines, we get perfect isolations, (i.e., $|s_{ij}| = 0$ for $i \leq 4, j \leq 4$) between all input ports.

3 Simulation of Results using Microstrip Transmission Line

The above ideal circuit cannot be directly translated to a microstrip circuit since in the layout we observe that the length of the crossover coupler is larger than the microstrip parallely present at the top and bottom. Hence, we attach bends and extra MLINS to compensate the length such the phase relation remains same.
We initially added TEEs to the circuit to avoid overlap of MLINs in the layout, however we weren't able to match the results obtained in the ideal circuit. So we didn't implement it in the final circuit.

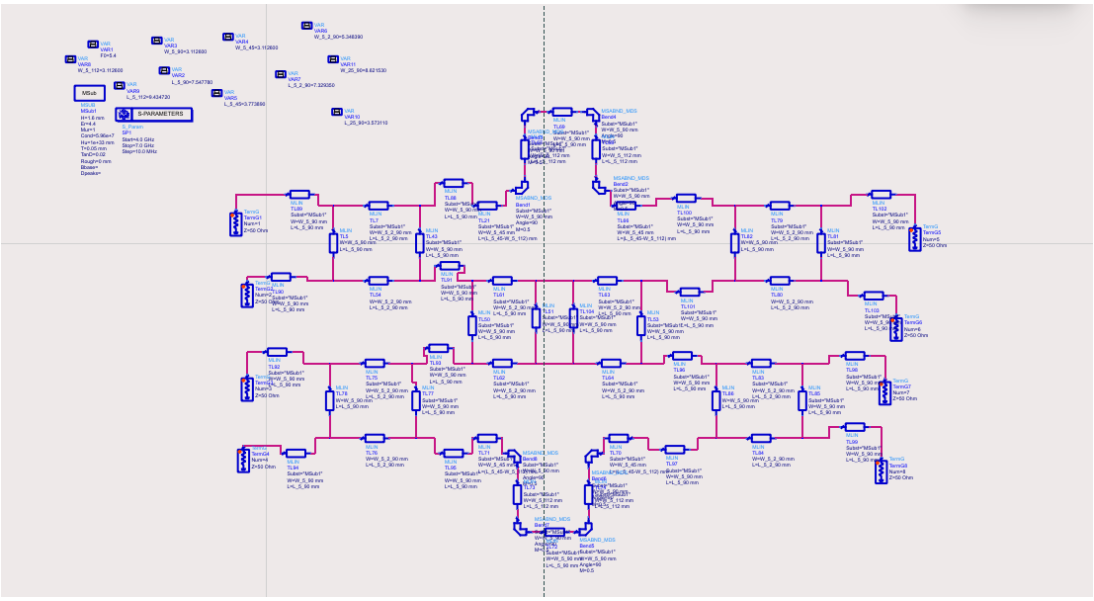


Figure 10: Schematic

Below, are the various simulation results using microstrip transmission lines.

3.1 Magnitude and Phase of s parameters between different Input and Output Ports

Using these plots, we can see the phase relations between the various input and output ports and the power division are similar to the ideal circuit.

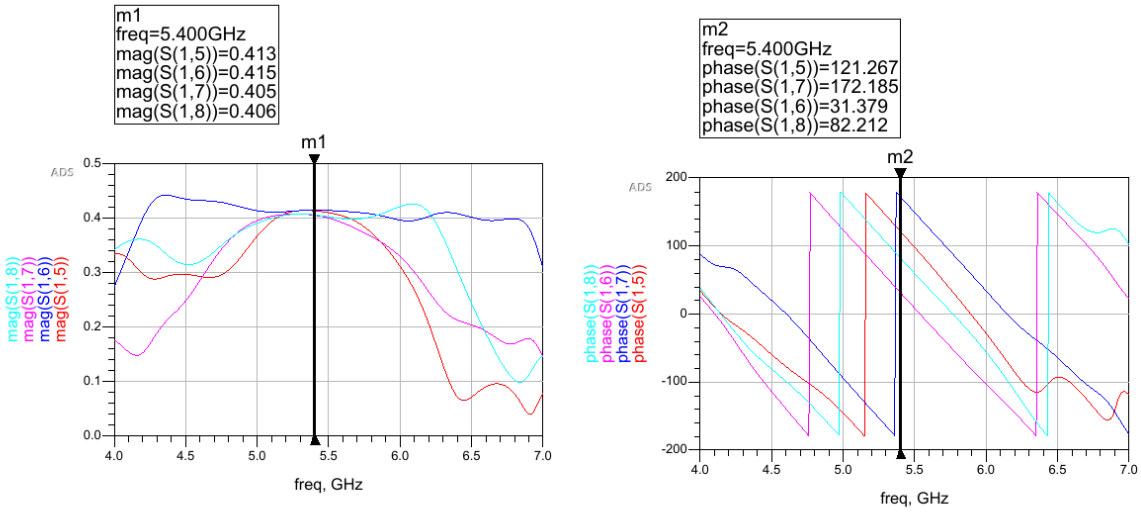


Figure 11: Input port 1

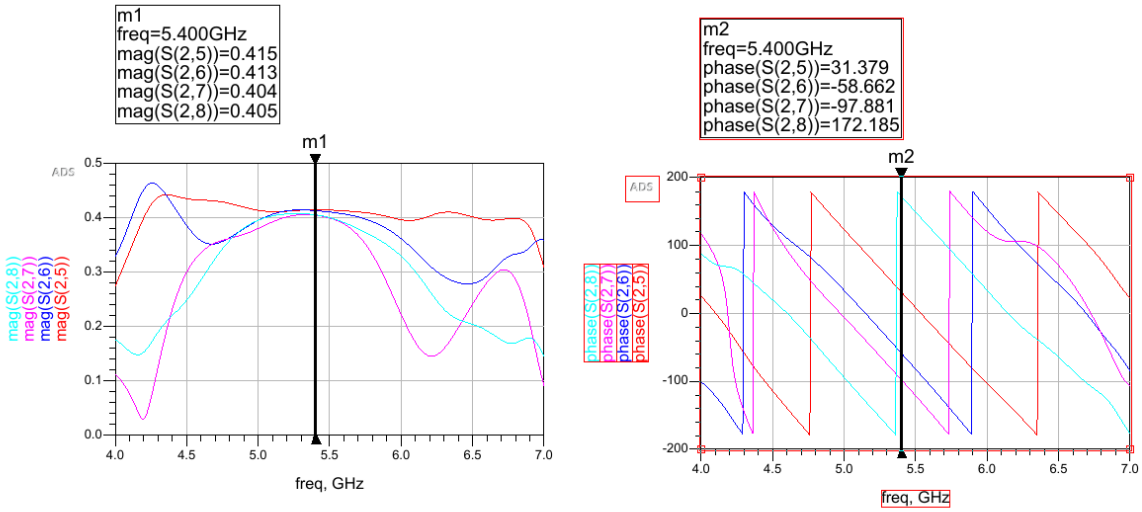


Figure 12: Input port 2

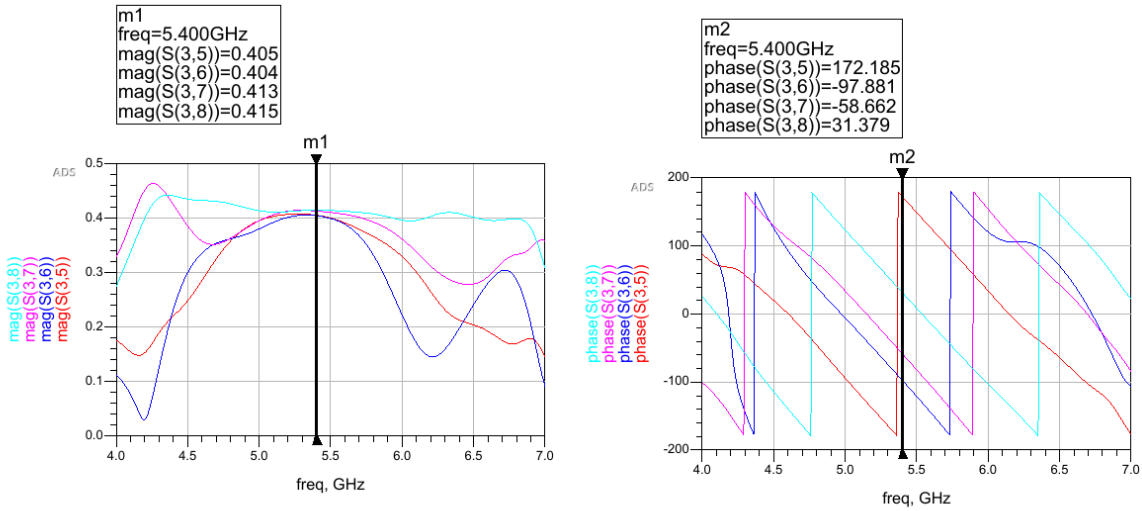


Figure 13: Input port 3

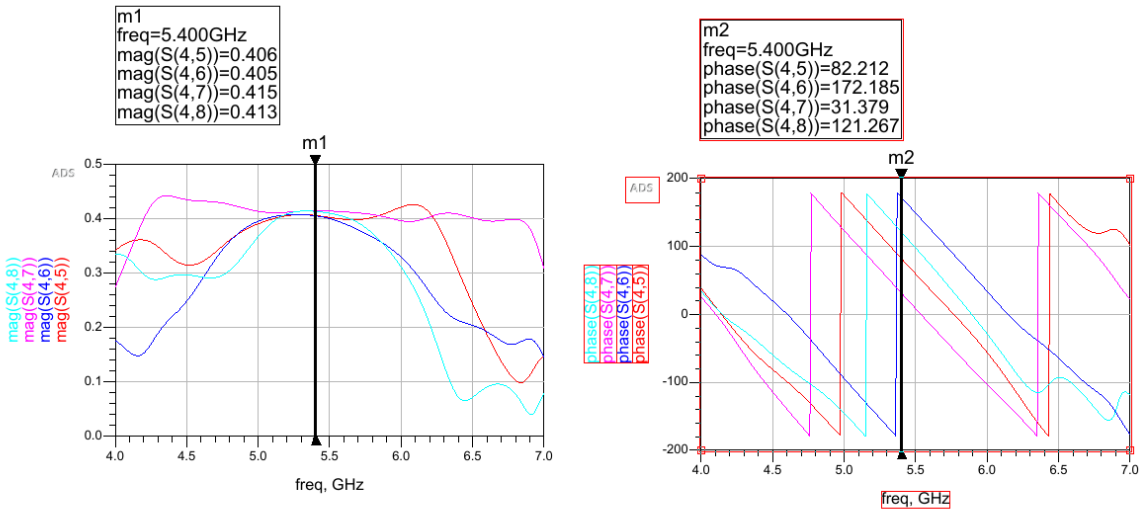


Figure 14: Input port 4

Since this is circuit is made using microstrip lines and other elements, we get power division of around around 0.4 from every input to every output port. Also, the phase relations obtained are slightly off. The circuit is a bit lossy because although each port has equal power division, some power is lost.

3.2 Magnitude and Phase of s parameters between Input ports

Using these plots, we can see the input ports are isolated from each other.

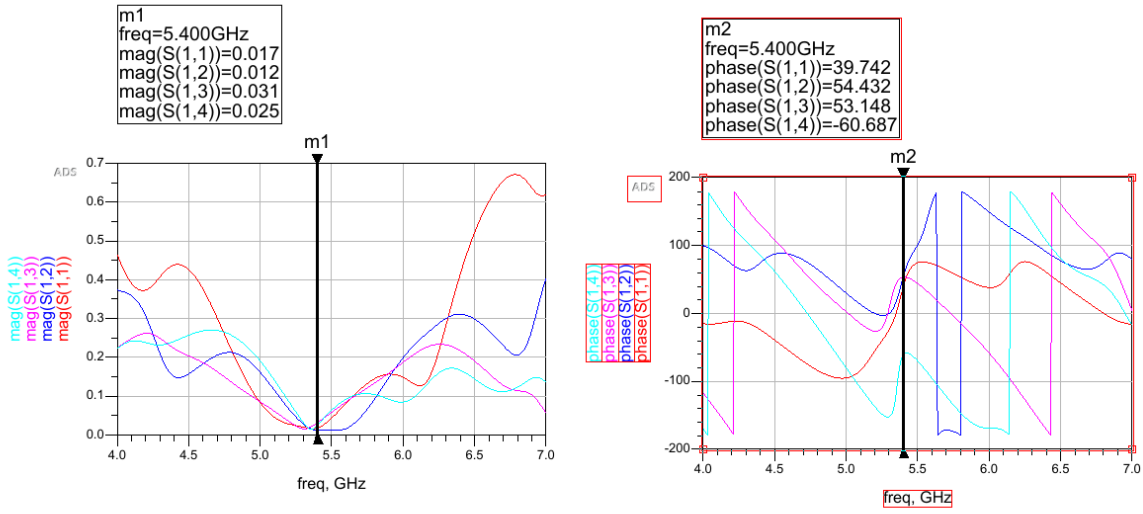


Figure 15: Input port 1

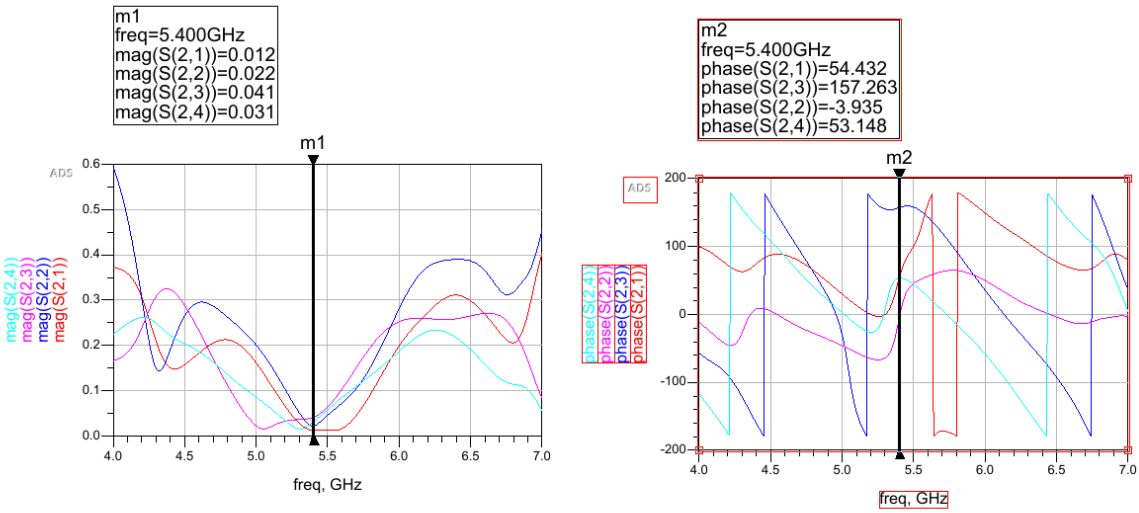


Figure 16: Input port 2

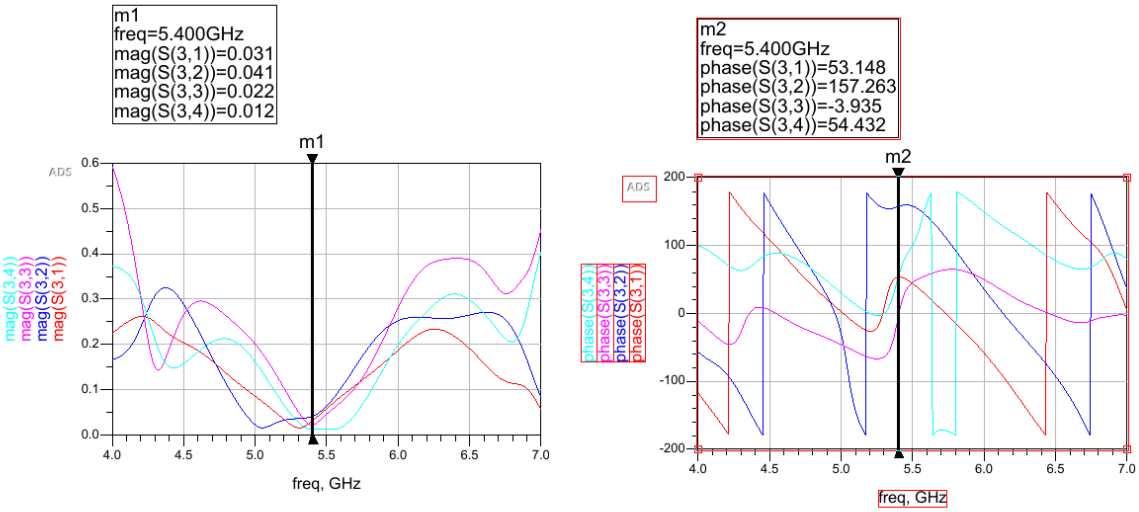


Figure 17: Input port 3

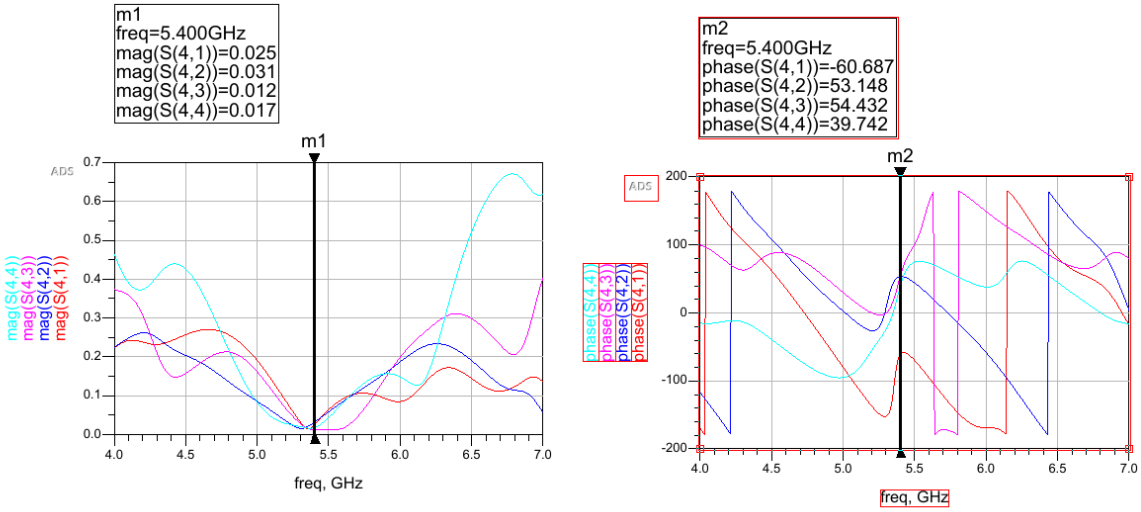


Figure 18: Input port 4

Although this circuit is made using microstrip lines, we still see good isolation between the input ports.

4 EM Simulation: Simulation of Layout

Since we didn't use TEEs we observe overlap between each MLIN. Hence, we were getting a matching at 6.279 GHz. To get the correct result we thus extend each MLIN such that the error due to overlap is nullified. We know that the frequency is inversely proportional to length. So we use the following relation to get the new length:

$$\frac{f_1}{f_2} = \frac{l_2}{l_1} = 1.16278$$

where, $f_2 = 6.279GHz$, $f_1 = 5.4GHz$. Thus, we multiply this factor with all the MLINs.

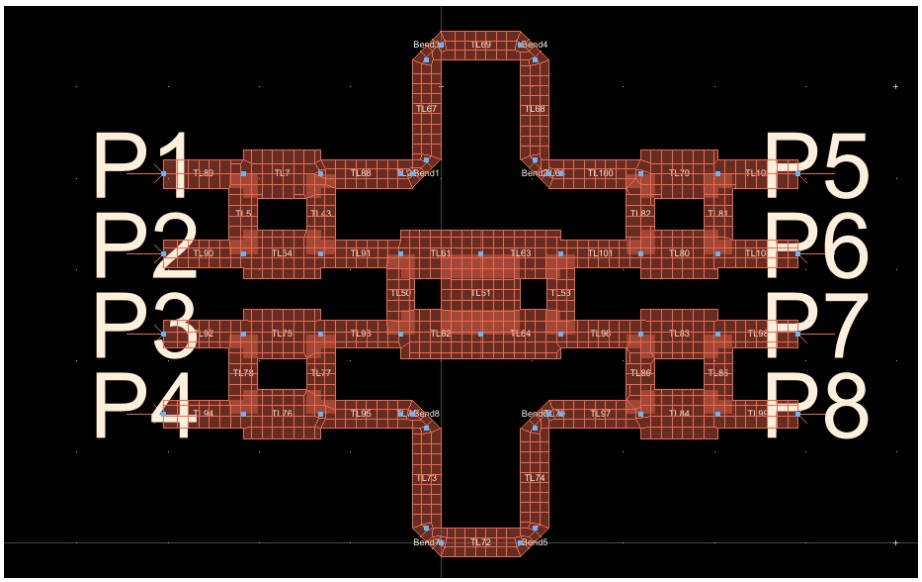


Figure 19: Layout

We then conduct EM simulation.

4.1 Magnitude and Phase of s parameters between different Input and Output Ports

Using these plots, we can see the phase relations between the various input and output ports and the power division are similar to the microstrip circuit.

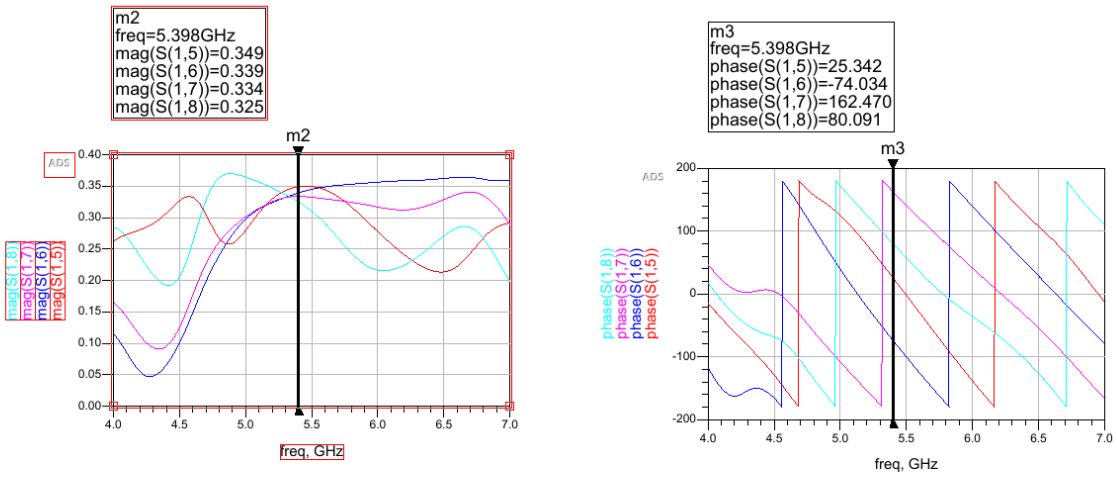


Figure 20: Input port 1

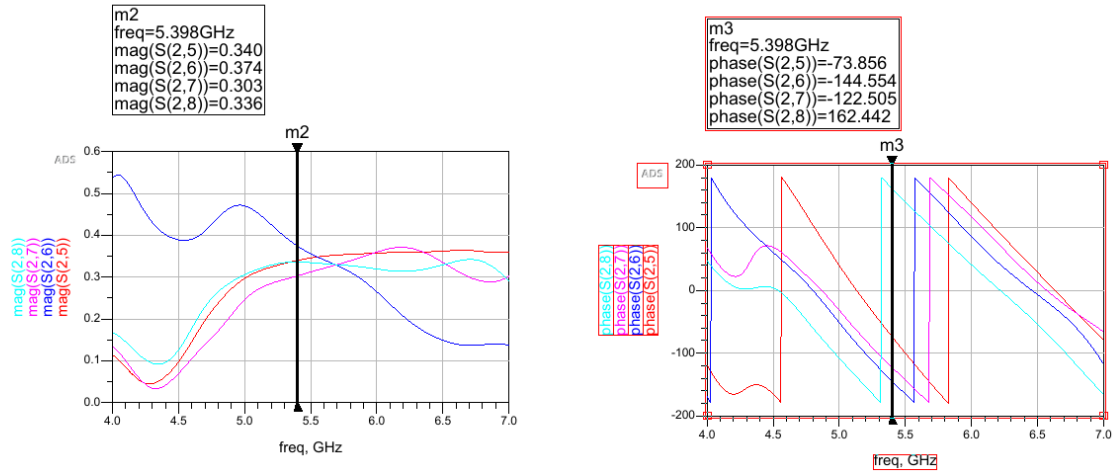


Figure 21: Input port 2

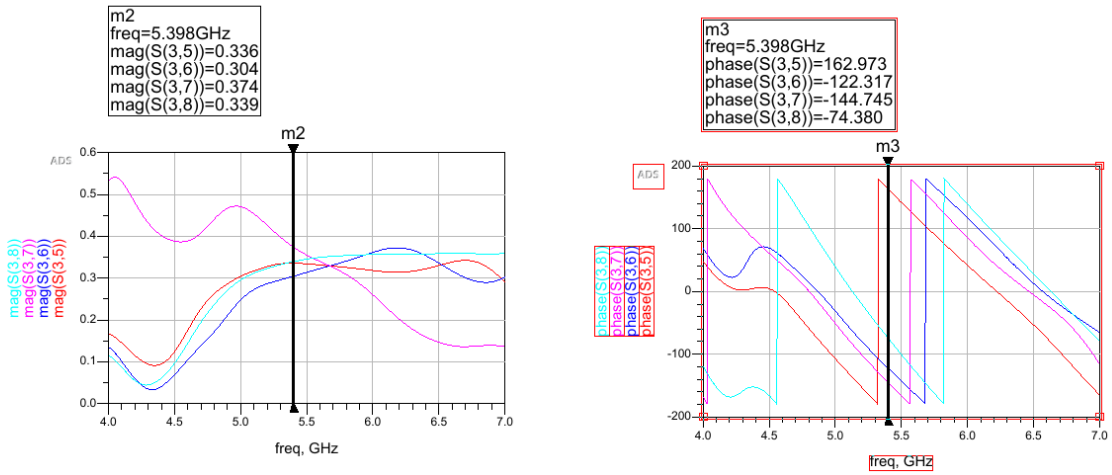


Figure 22: Input port 3

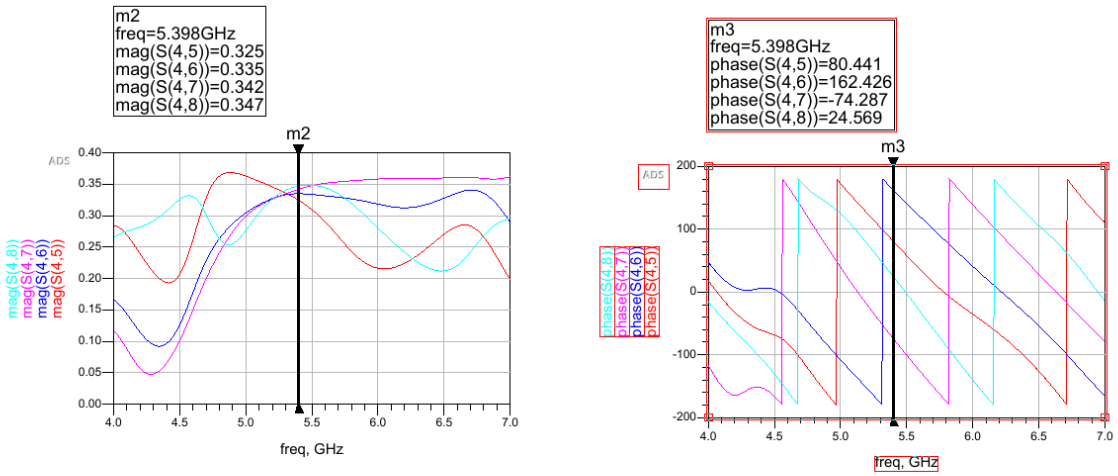


Figure 23: Input port 4

We see almost equal power division between different input and output ports, although it's more lossy now.

4.2 Magnitude and Phase of s parameters between Input ports

Using these plots, we can see the input ports are isolated from each other.

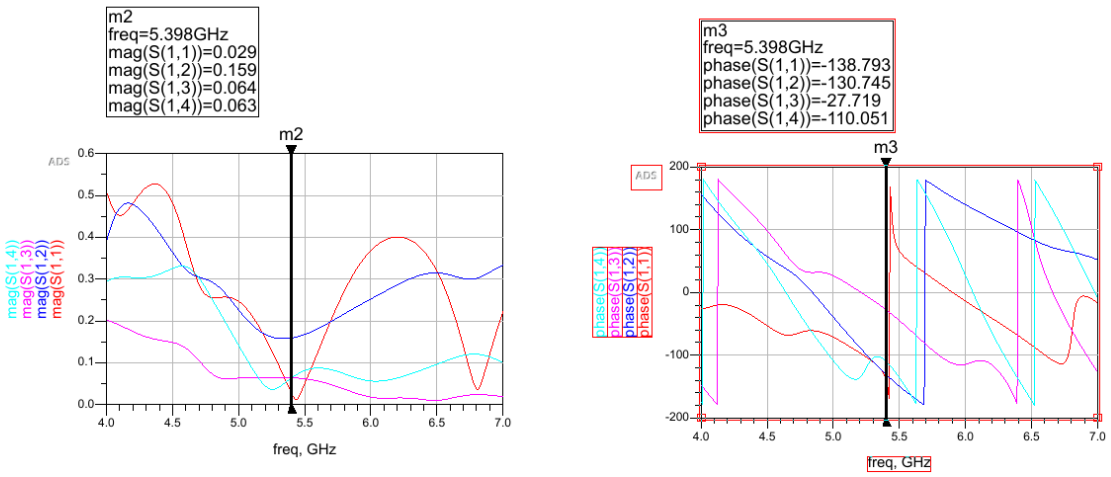


Figure 24: Input port 1

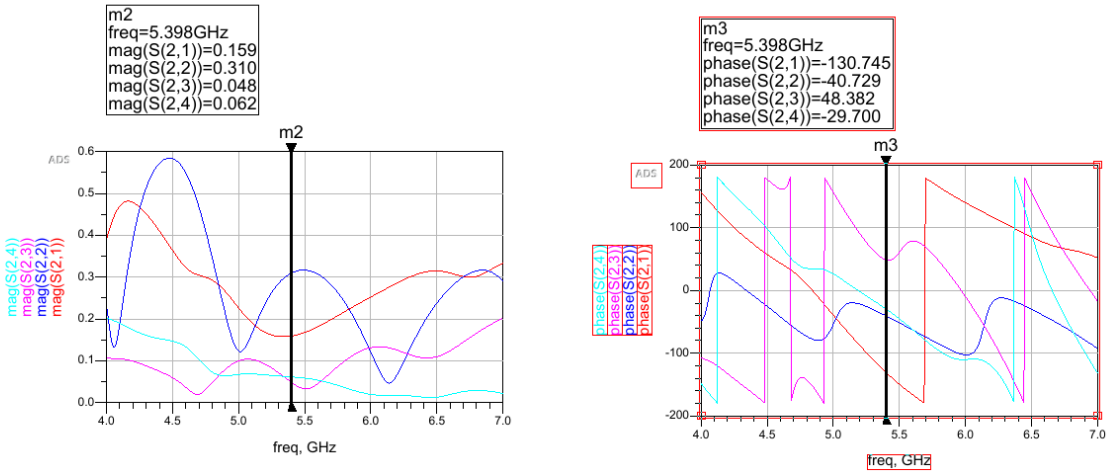


Figure 25: Input port 2

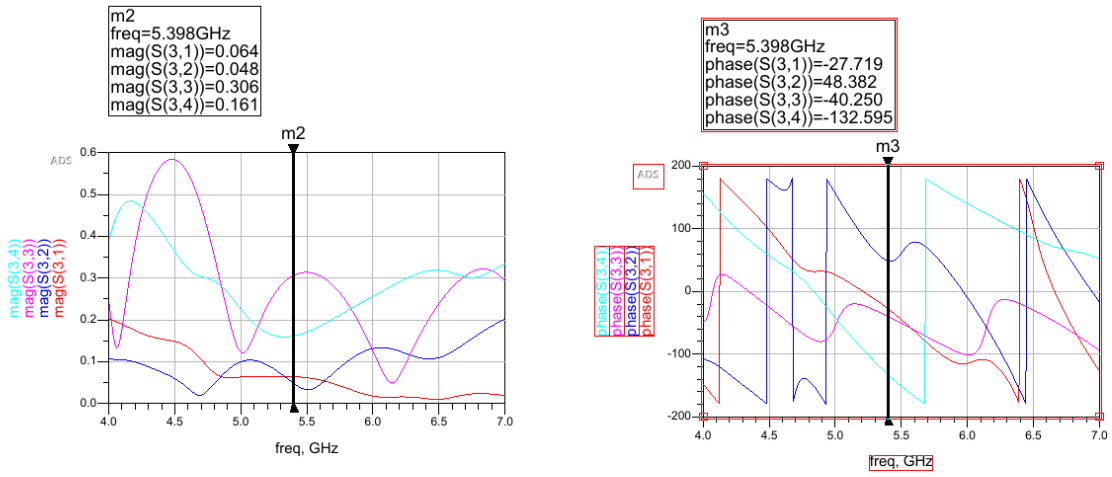


Figure 26: Input port 3

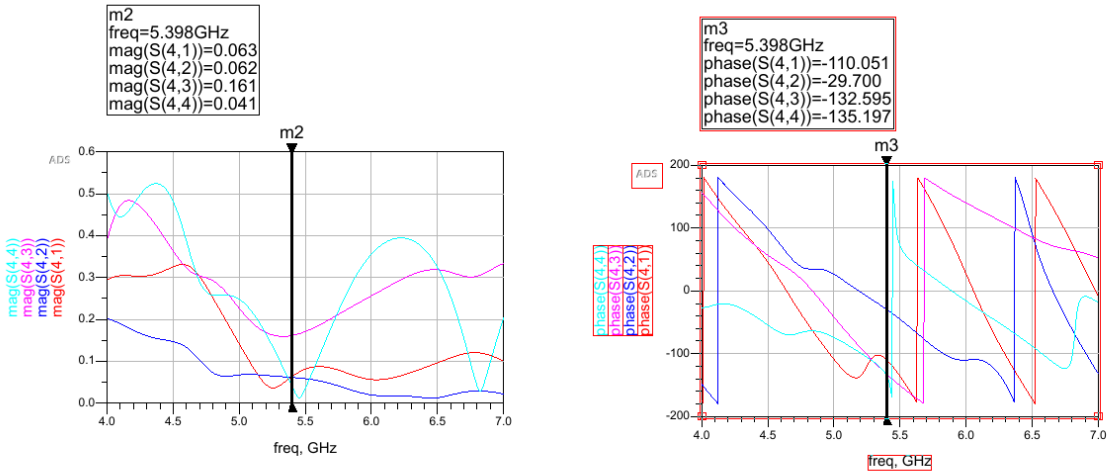


Figure 27: Input port 4

5 Final Fabricated Circuit

We printed the layout on butter paper and give it in the PCB lab for fabrication. Here is our fabricated and soldered PCB:

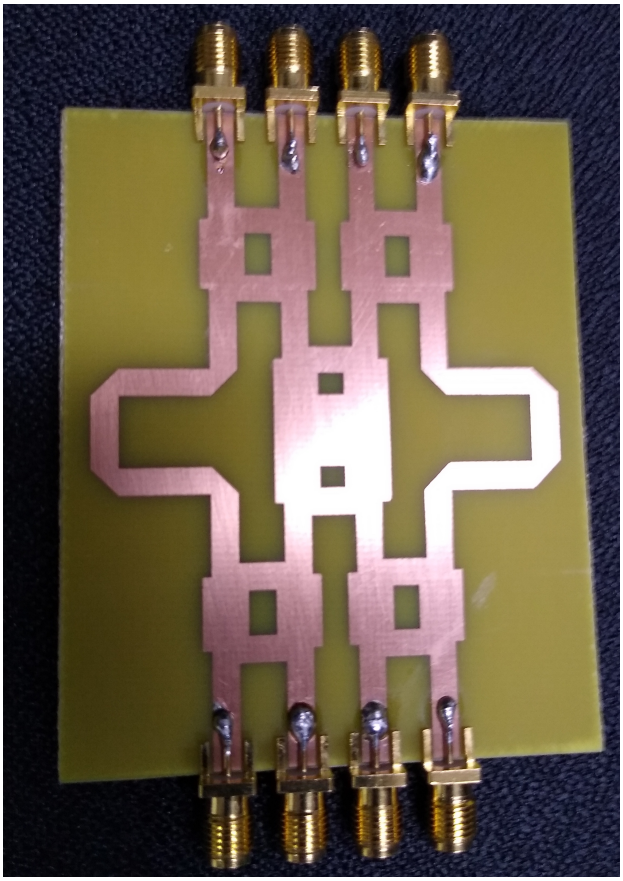


Figure 28: Final Fabricated Circuit

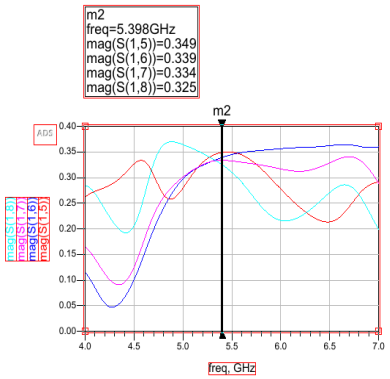
Figure 29: Final Fabricated Circuit

We then conduct measurements. Our measurement results are as follows:

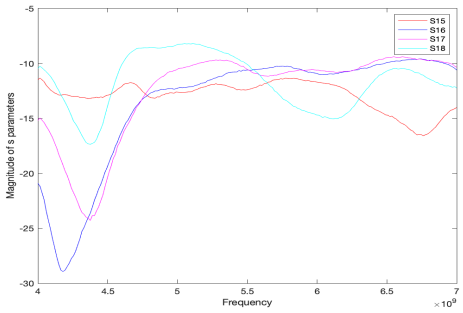
5.1 Magnitude and Phase of s parameters between different Input and Output Ports

Using these plots, we can see the phase relations between the various input and output ports are similar to layout results and the power is divided equally between input and output ports.

Simulation

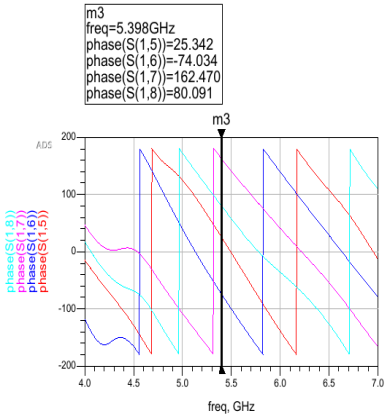


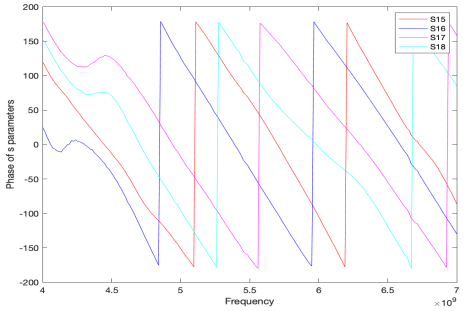
Measured (dB)



Input port 1

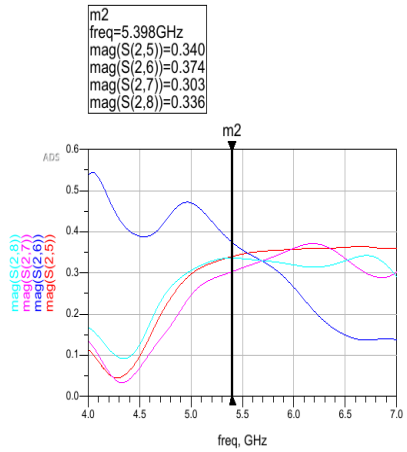
Magnitude

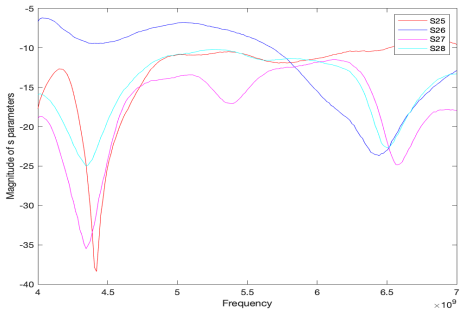




Input port 1

Phase



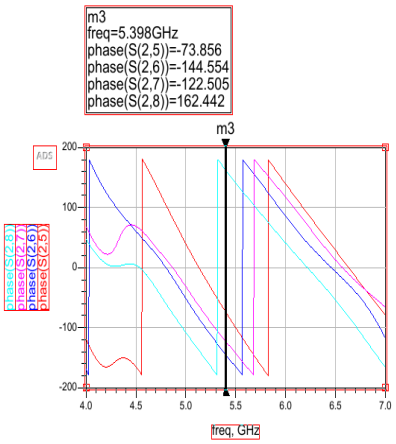


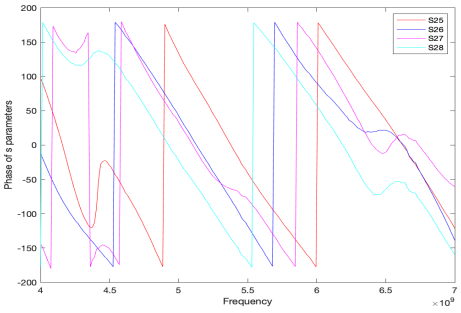
Input port 2

Magnitude

Simulation

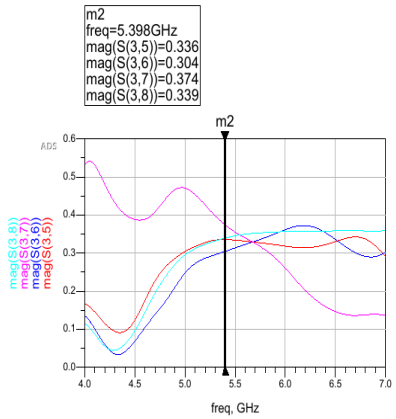
Measured (dB)

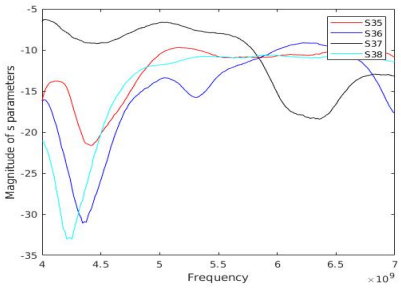




Input port 2

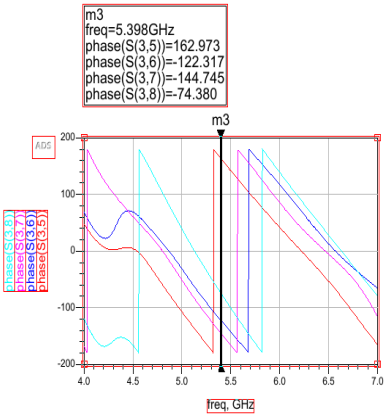
Phase

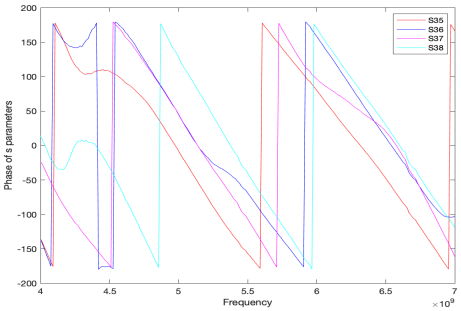




Input port 3

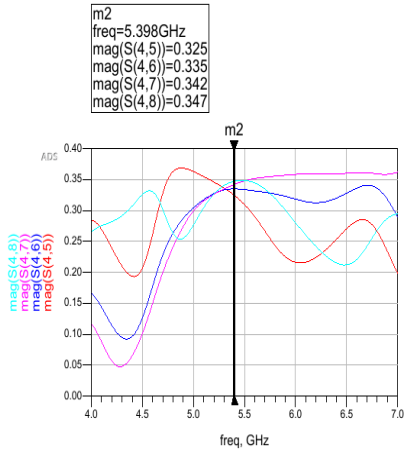
Magnitude

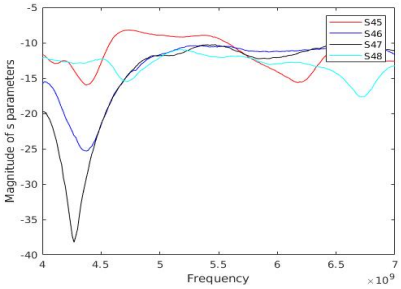




Input port 3

Phase

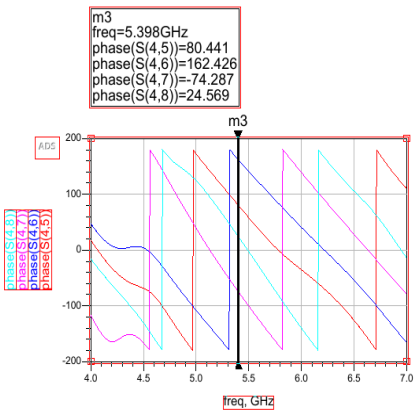




Input port 4

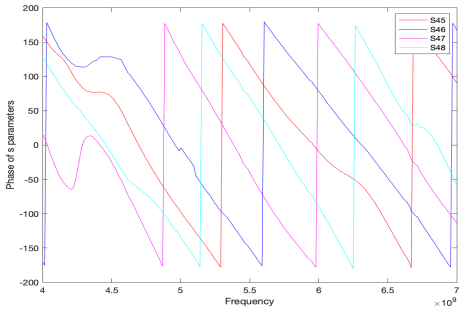
Magnitude

Simulation



Input port 4

Measured (dB)



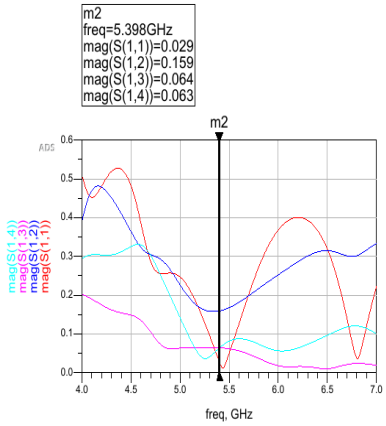
Phase

We see almost equal power division between different input and output ports, although it's more lossy now.

5.2 Magnitude and Phase of s parameters between Input ports

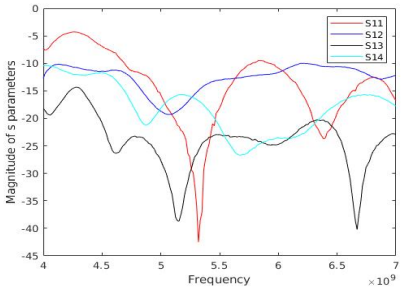
Using these plots, we can see the input ports are isolated.

Simulation



Input port 1

Measured (dB)



Magnitude