Power Amplifier

EE614 : Project Report

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Specifications:

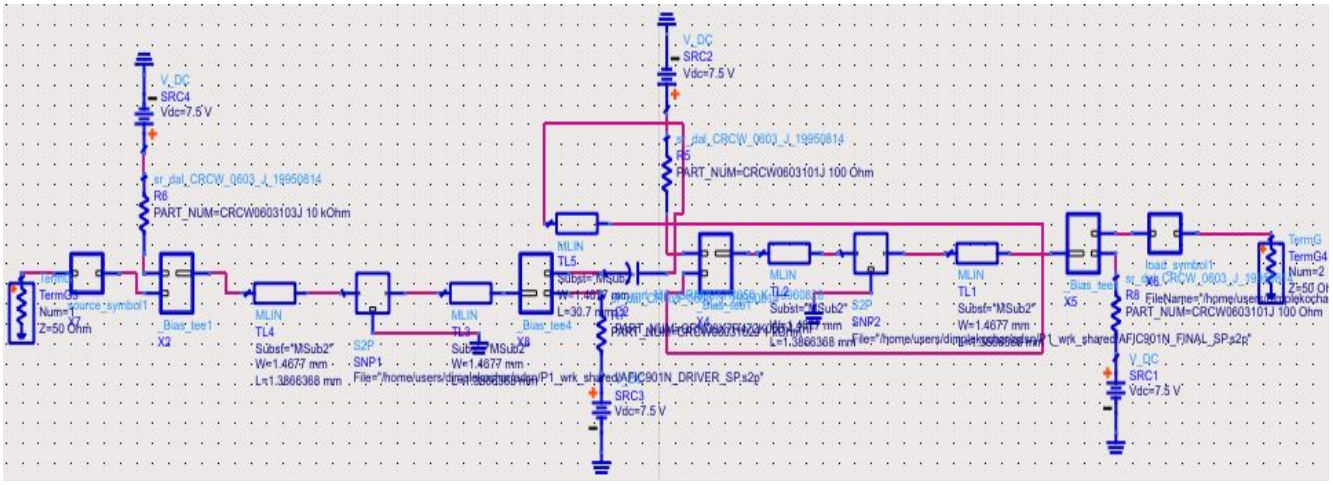
1. A power amplifier using AFIC901N for a gain of at least 20 dB at 520 MHz
2. The amplifier should have S 11 and S 12 values less than -10 dB and -60 dB respectively

Parameters considered while designing:

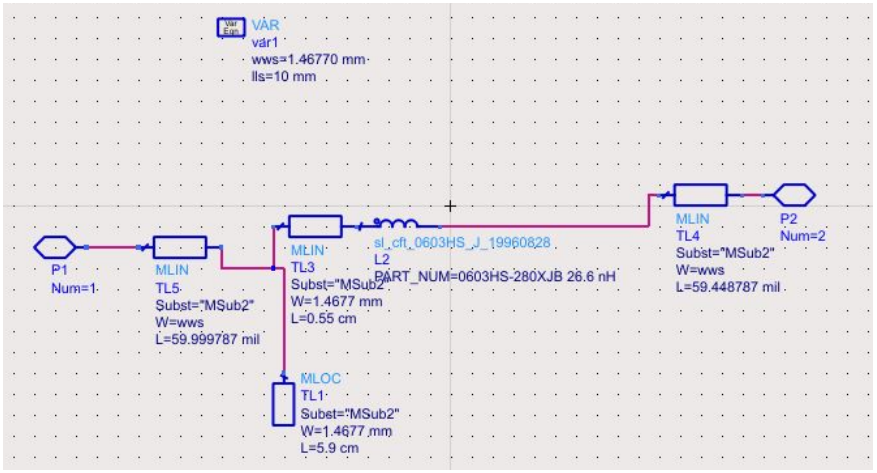
1. Gain
2. Input and Output Matching
3. Stability
4. Biasing

Schematics:

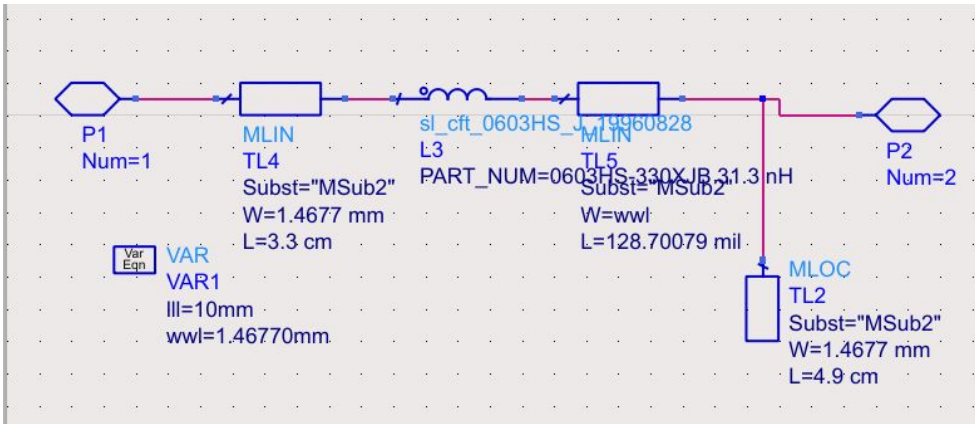
(i)Complete schematic:



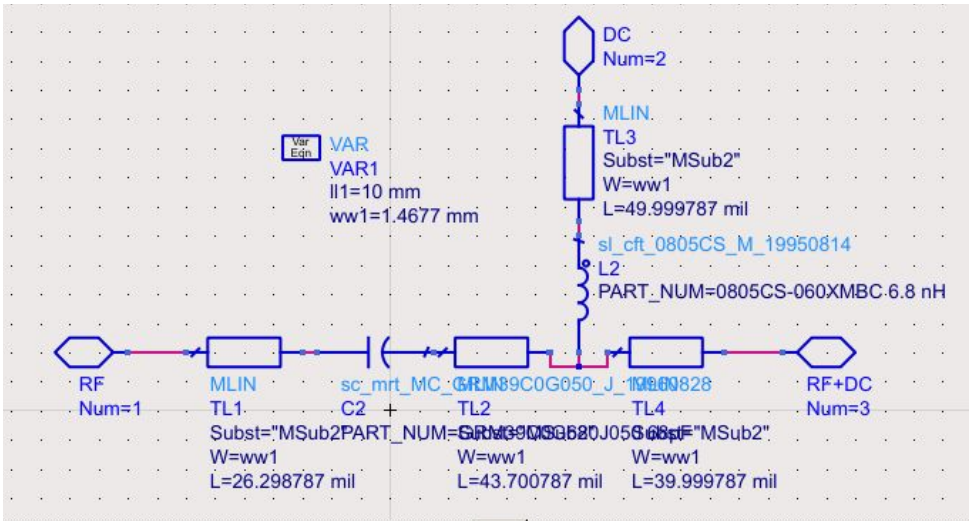
(ii)Source Symbol Schematic:



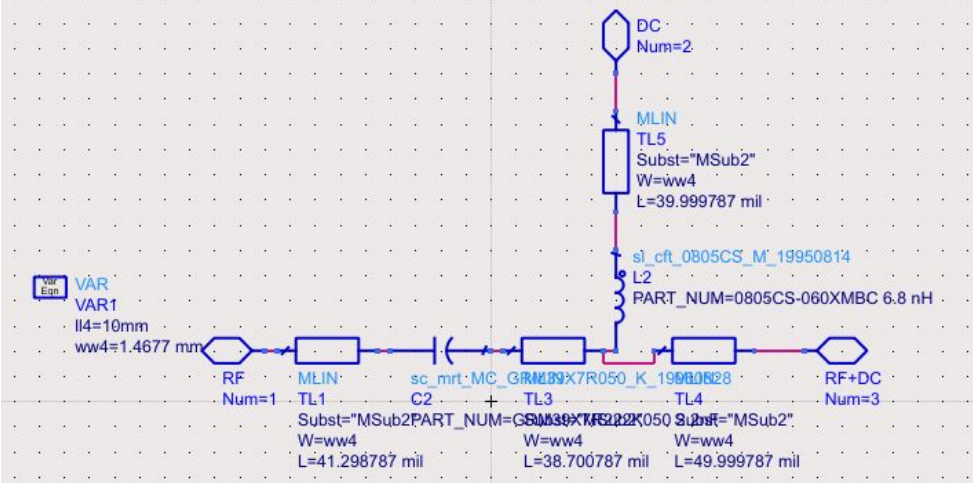
(iii)Load Symbol Schematic:



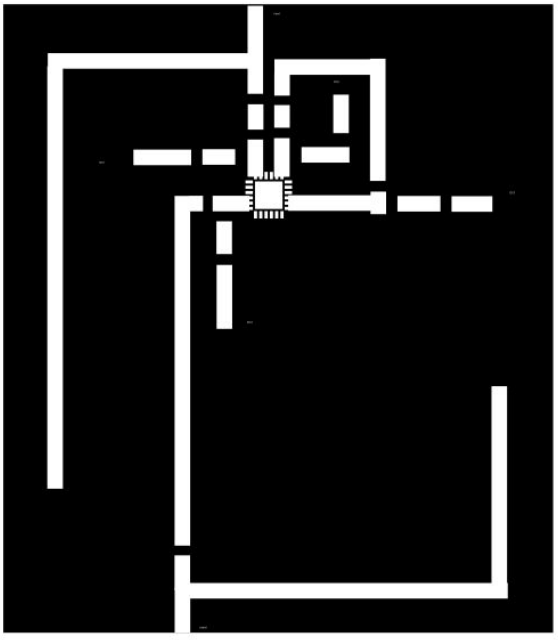
(iv) Bias tee at source:



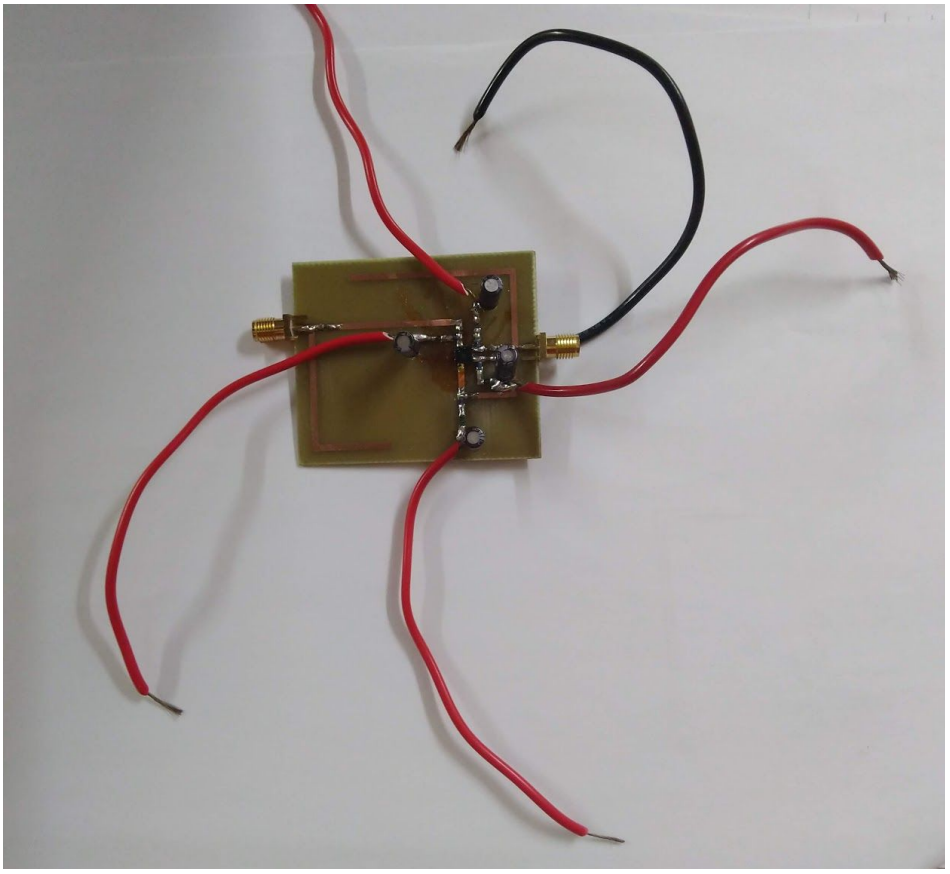
(v) Bias tee at the load:



Layout:

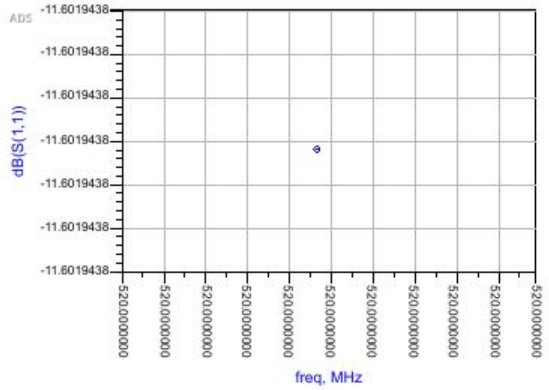


Final PCB with smds and SMA connectors:



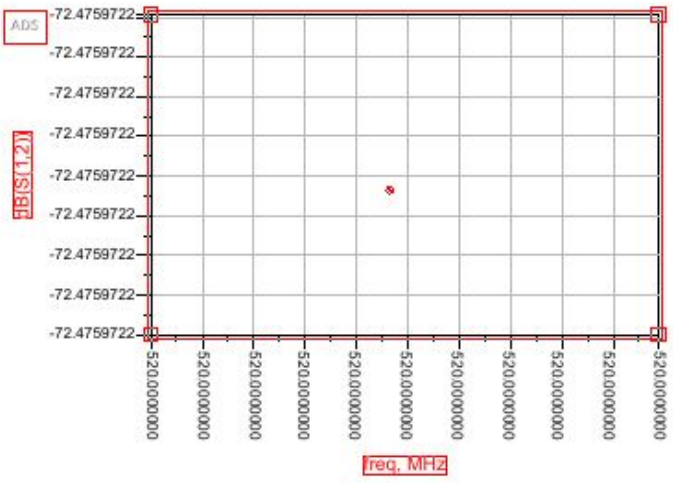
Simulation Results:

(i)S_11:

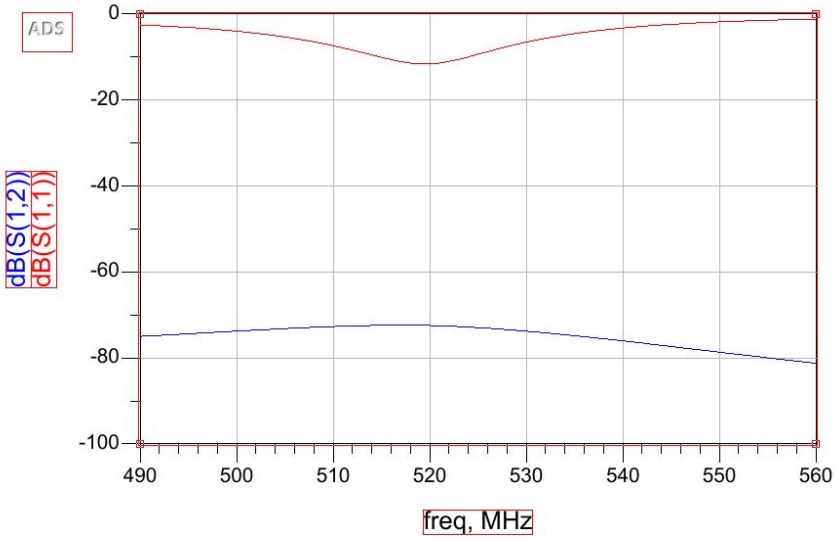


It is around -11.6dB which is less than -10dB meeting the requirement

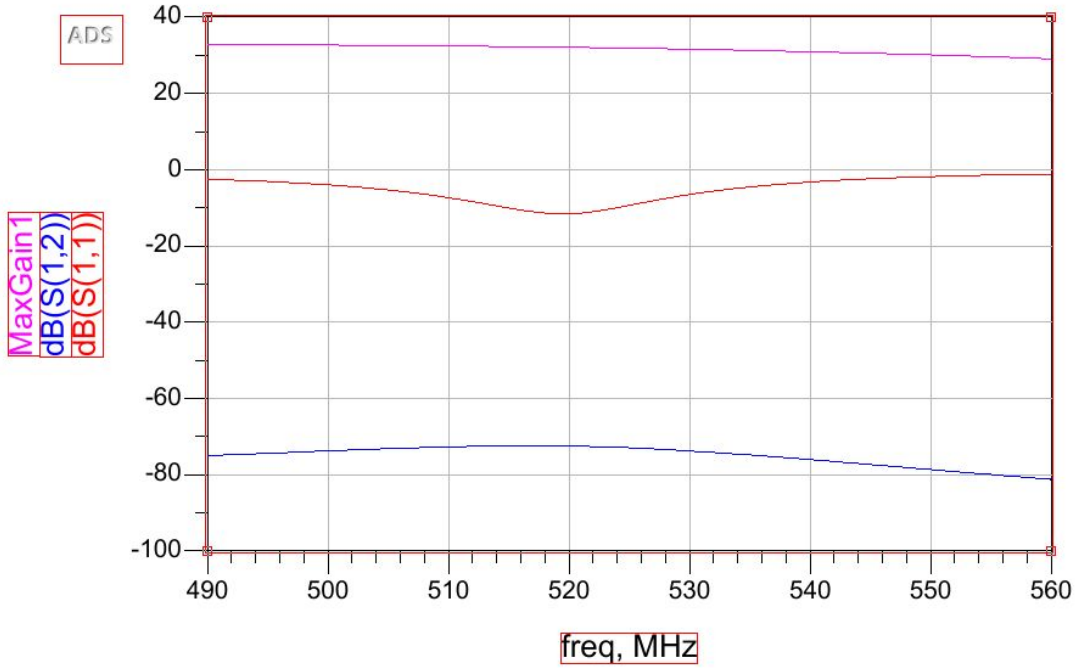
(ii)S_12:



It is around -72.4dB which is less than -60dB meeting the requirement

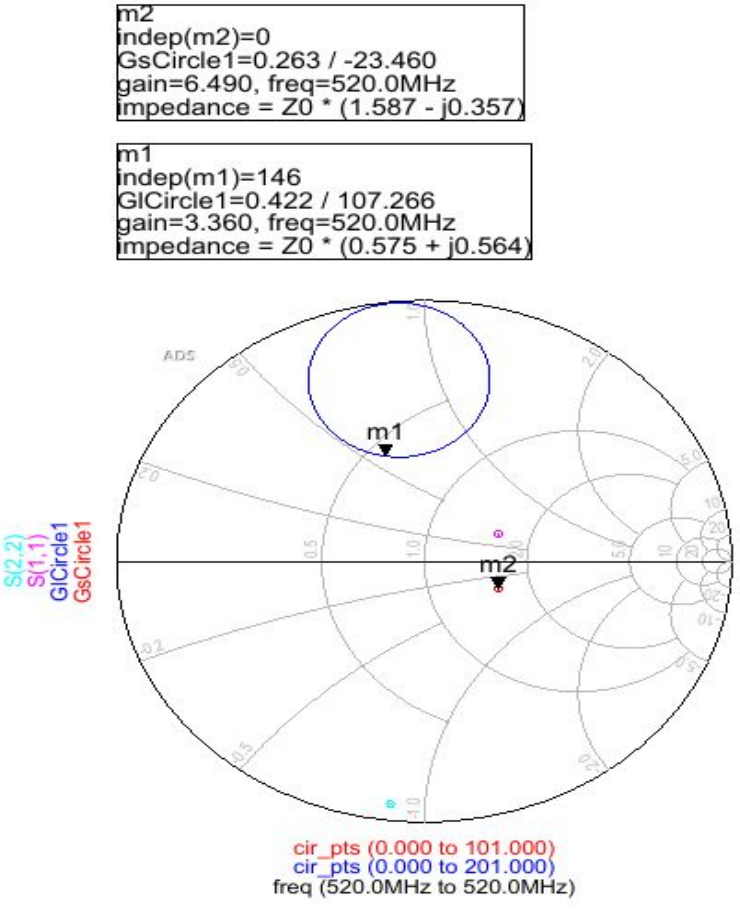


(iii) Frequency plot of S_11, S_12, Gain:



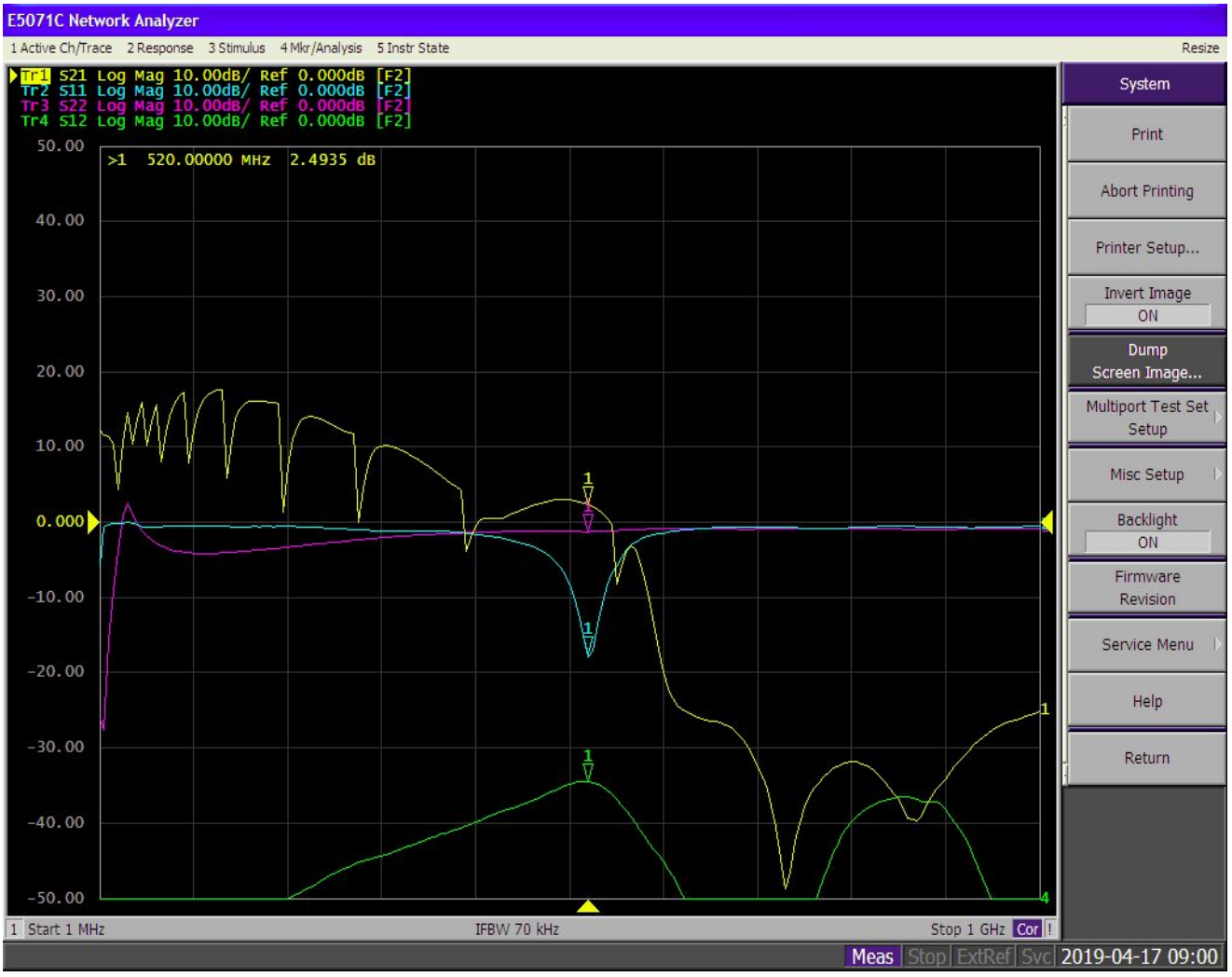
We can conclude from the plot that the gain is greater than 20 dB for all frequencies

(iv)Gain circles:



PCB Testing Results:

On verifying the results on Vector Network Analyzer EE5071c we get the following plot:



At 520 MHz we were getting a gain of 2.4935 dB.

Challenges in schematic and biasing

1. How to approach
2. We thought we'd be able to satisfy the constraints using matching but we had to tune components independently to satisfy the constraint on s11
3. Tuning the components such that the values are realisable
4. Biasing the components in order to satisfy the constraints such as the required current