EE 671: Assignment 4 Report
16 bit Brent Kung Adder

Dimple Kochar, 16D070010

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Directory: /home/courseusers/EE671/EE671_15
In this directory, library assign4 has all the files.

1 Order of figures for each module

1. Schematic of individual modules, whole 16 bit Brent Kung adder and their particular test benches.
2. Simulation results for the individual modules and whole adder.
3. The layout of individual modules and whole adder.
4. DRC and LVS report of individual modules and whole adder.
5. Post layout simulation results (In environment we append calibre, where calibre view was generated after pex of layout) for the individual modules and whole adder.

1.1 Inverter/NOT gate: (NOT)

1.

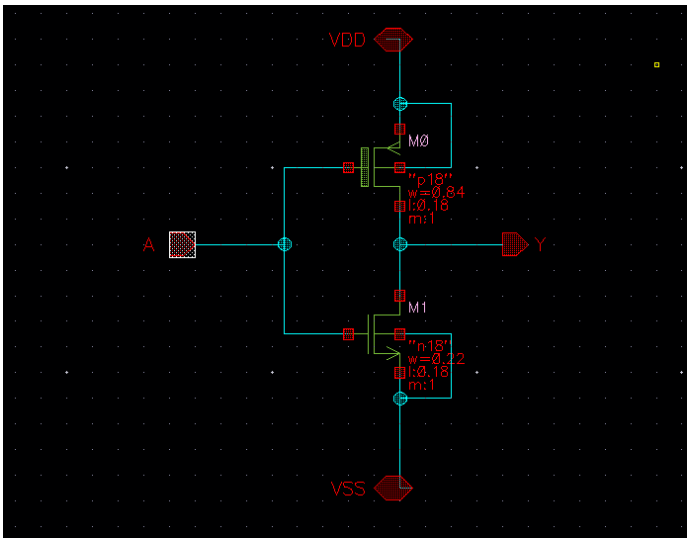

Figure 1: Schematic of NOT

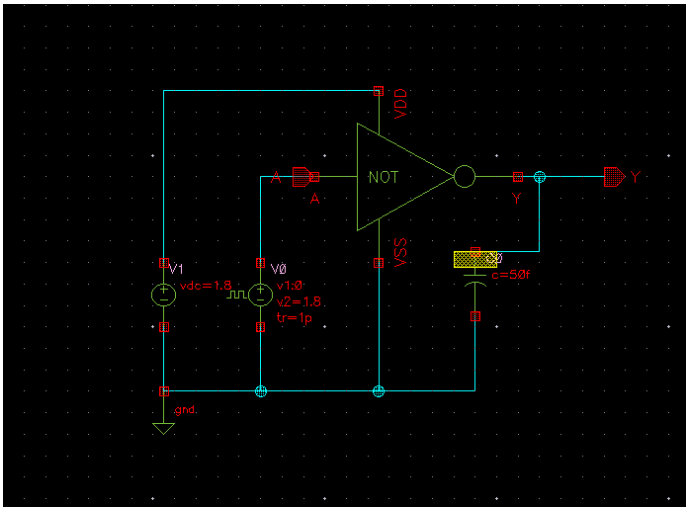

Figure 2: Schematic of NOT_test

2.

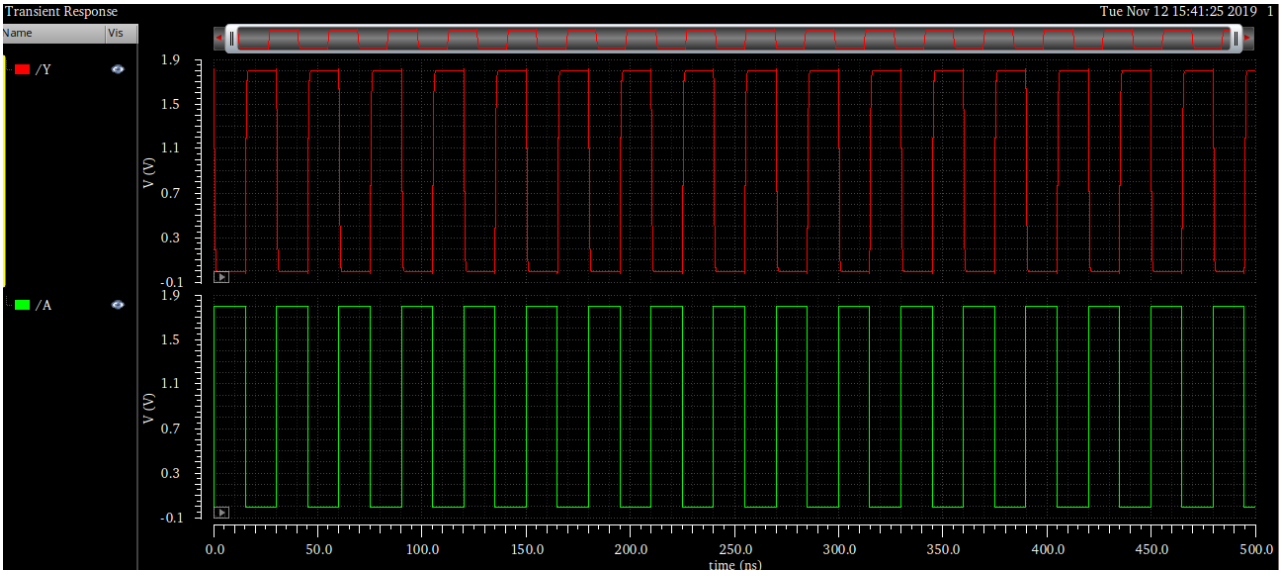

Figure 3: Simulation result of Schematic

3.

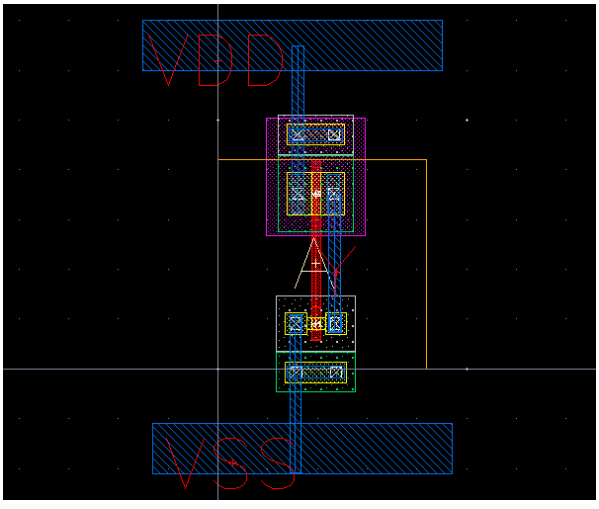

Figure 4: Layout of NOT

4.

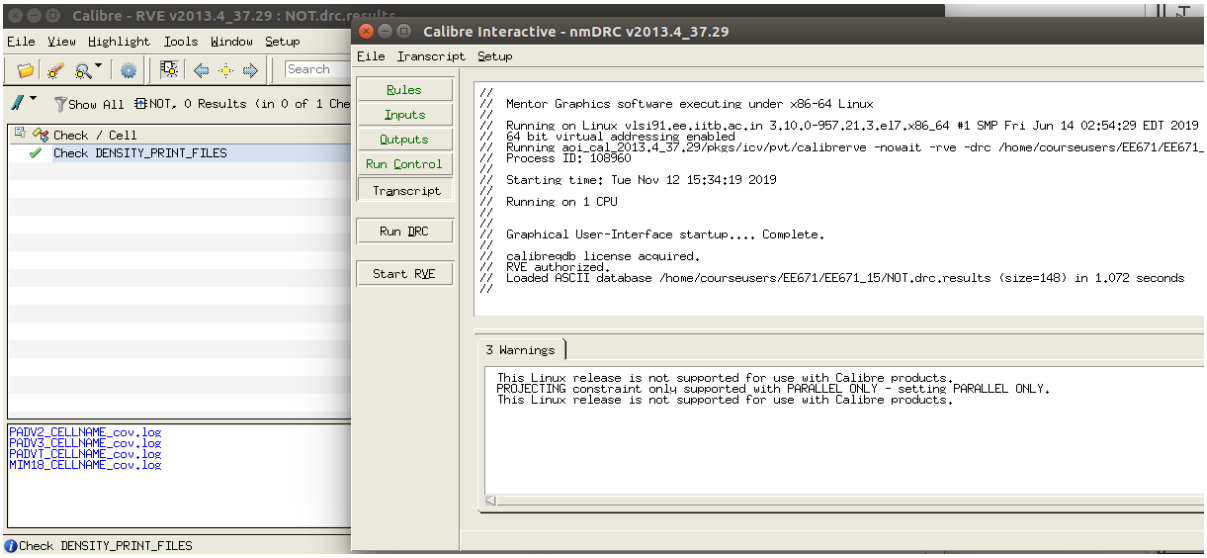

Figure 5: DRC of NOT

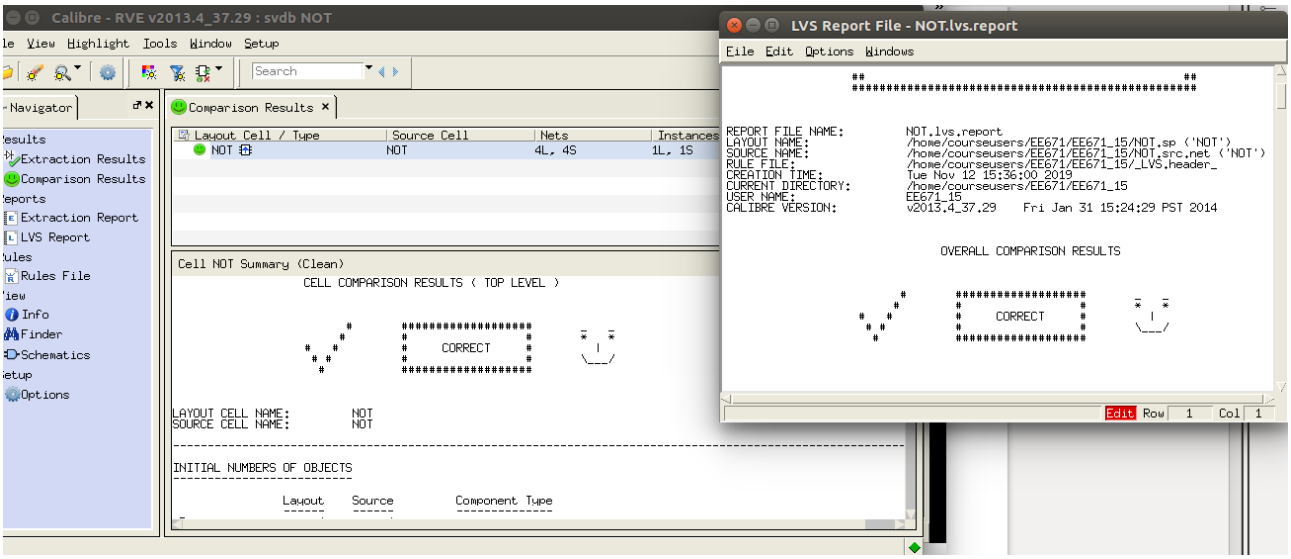

Figure 6: LVS of NOT

5.

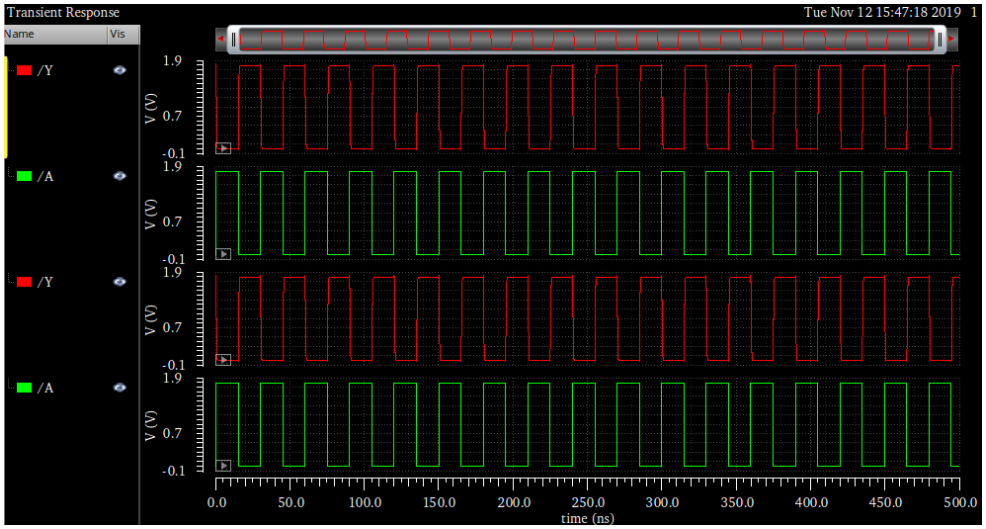

Figure 7: Simulation result of Layout

1.2 NAND gate: (NAND)

1.

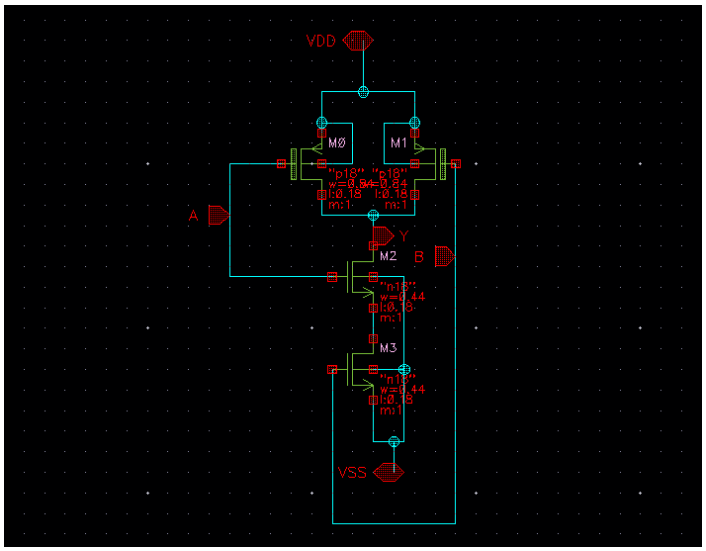

Figure 8: Schematic of NAND

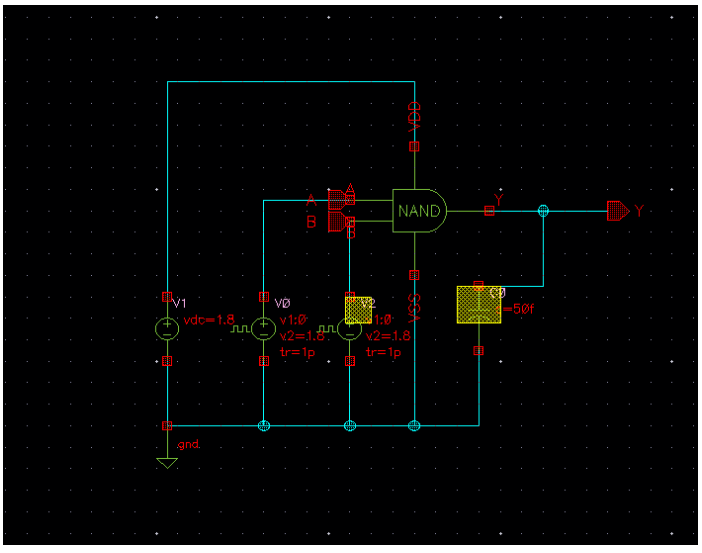

Figure 9: Schematic of NAND_test

2.

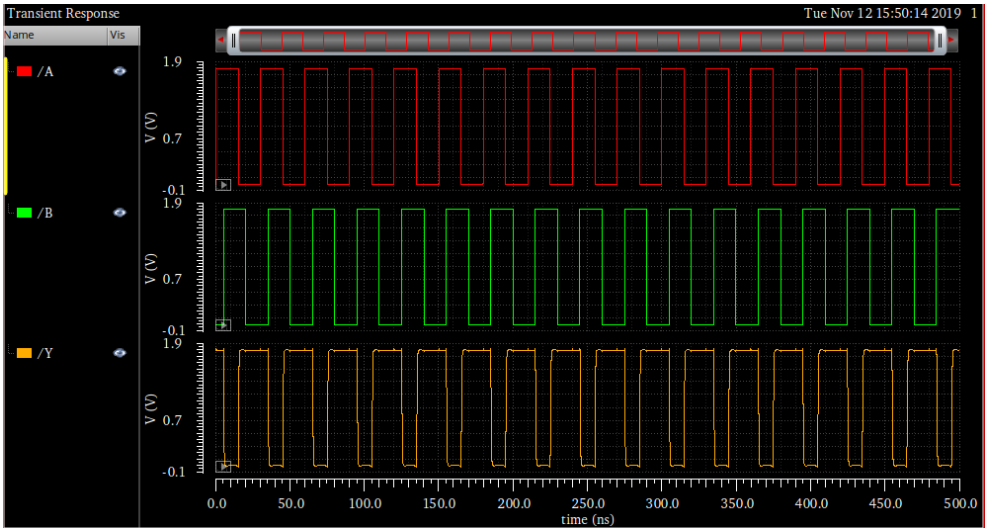

Figure 10: Simulation result of Schematic

3.

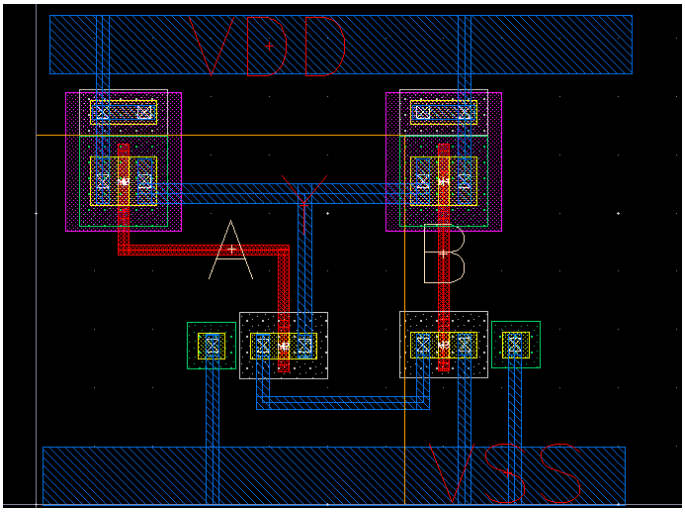

Figure 11: Layout of NAND

4.

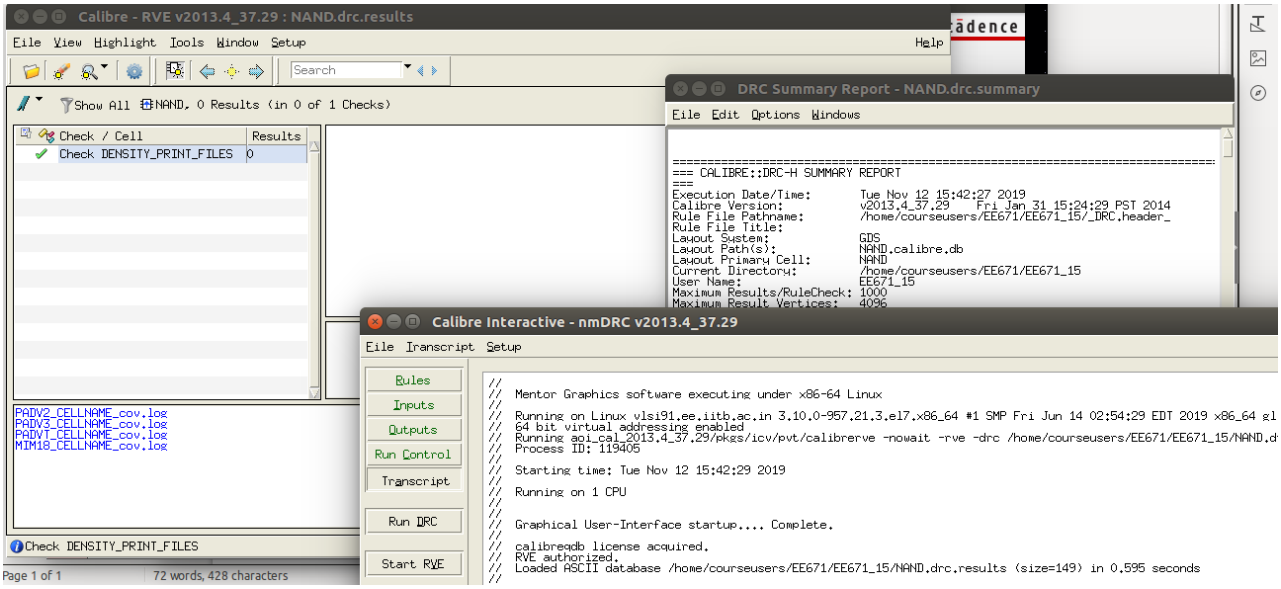

Figure 12: DRC of NAND

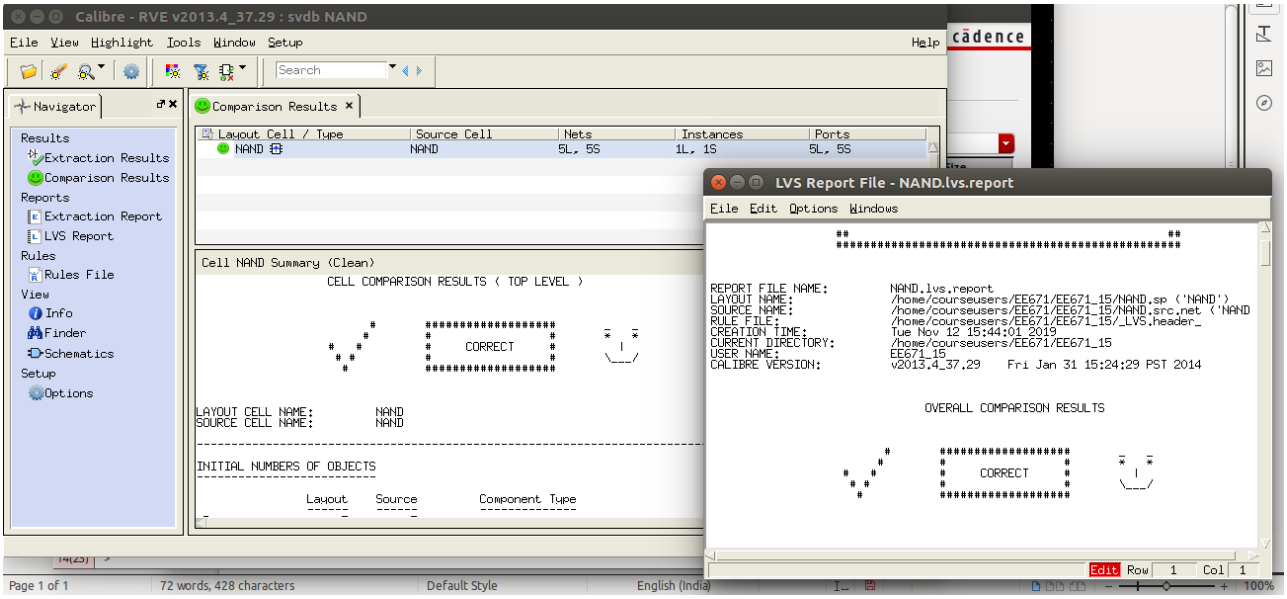

Figure 13: LVS of NAND

5.

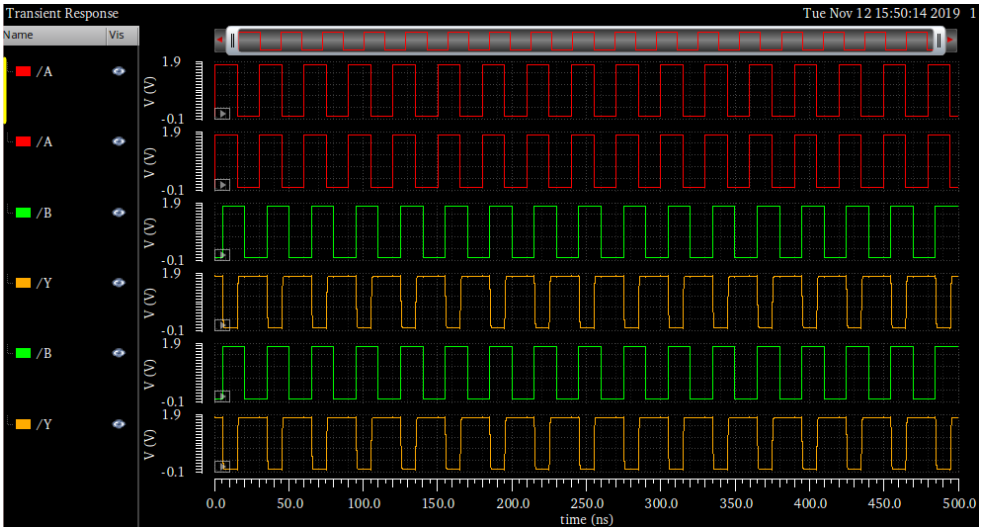

Figure 14: Simulation result of Layout

1.3 AND gate: (AND)

1.

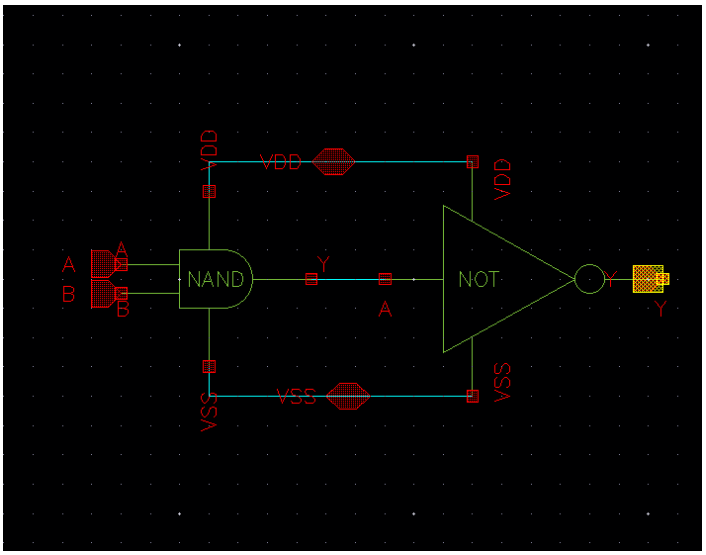

Figure 15: Schematic of AND

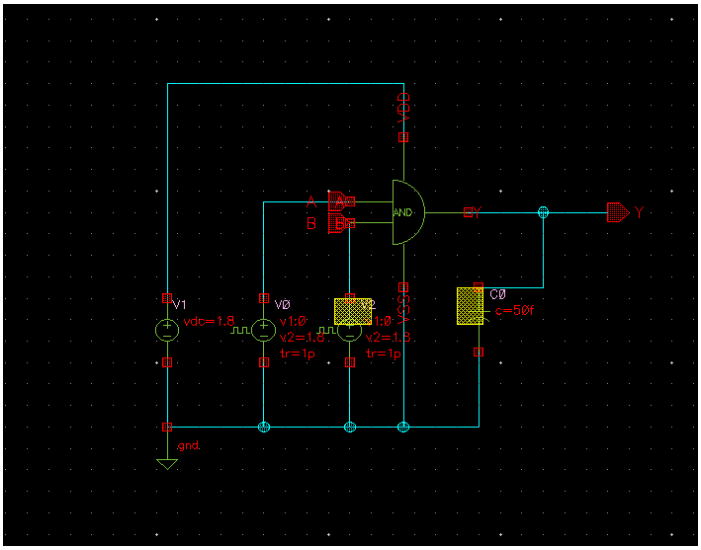

Figure 16: Schematic of AND_test

2.

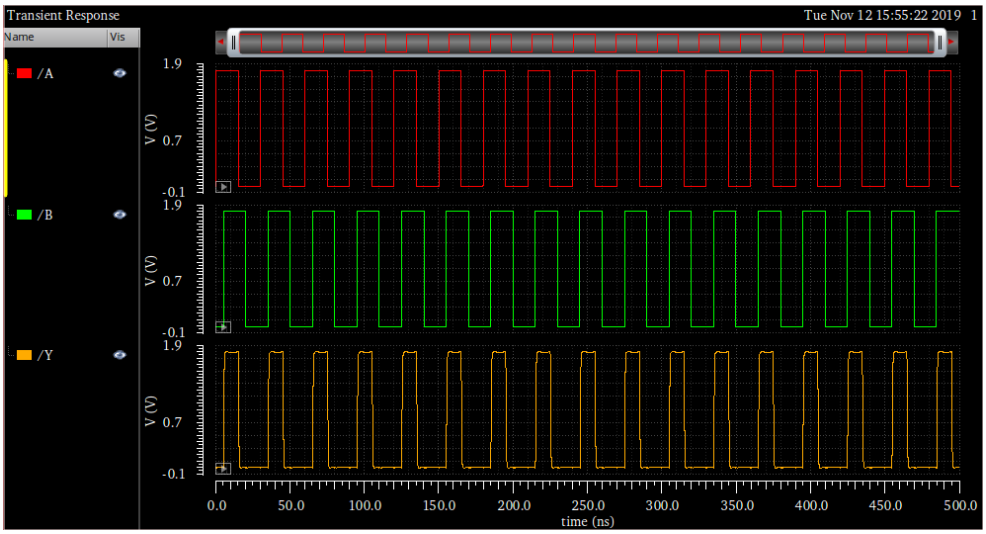

Figure 17: Simulation result of Schematic

3.

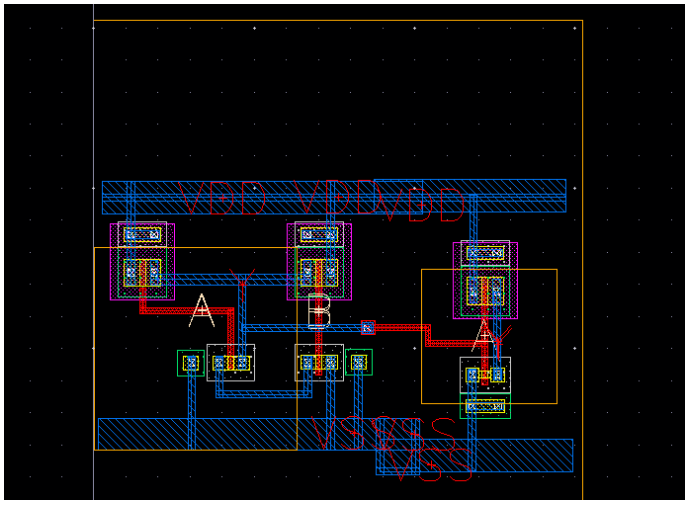

Figure 18: Layout of AND

4.

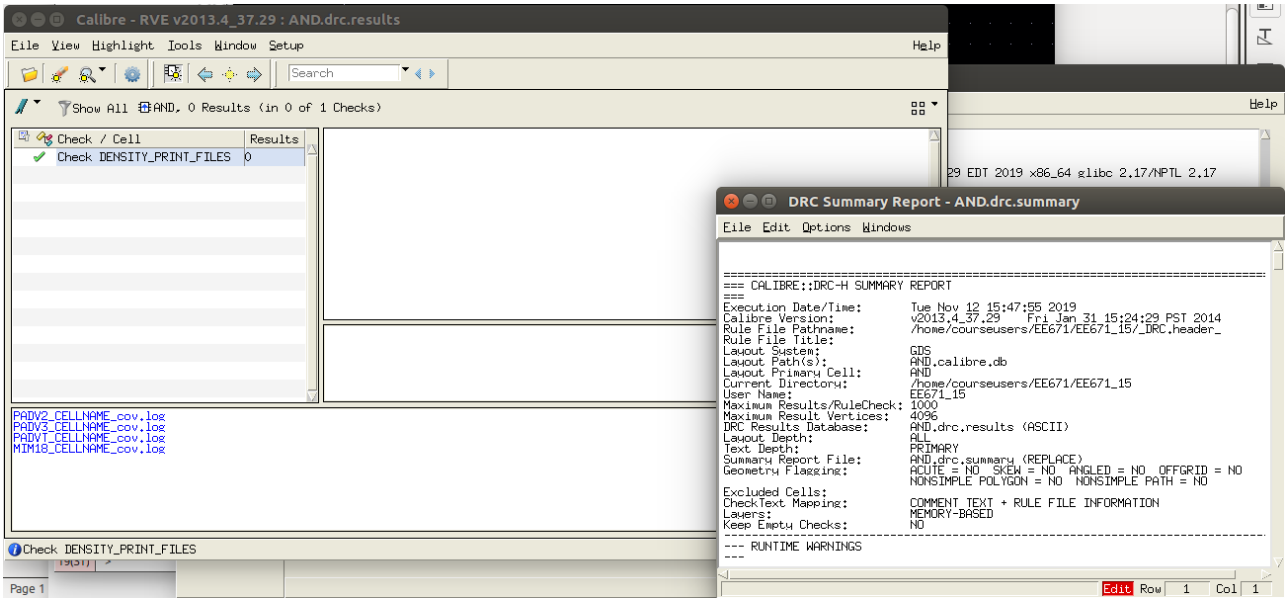

Figure 19: DRC of AND

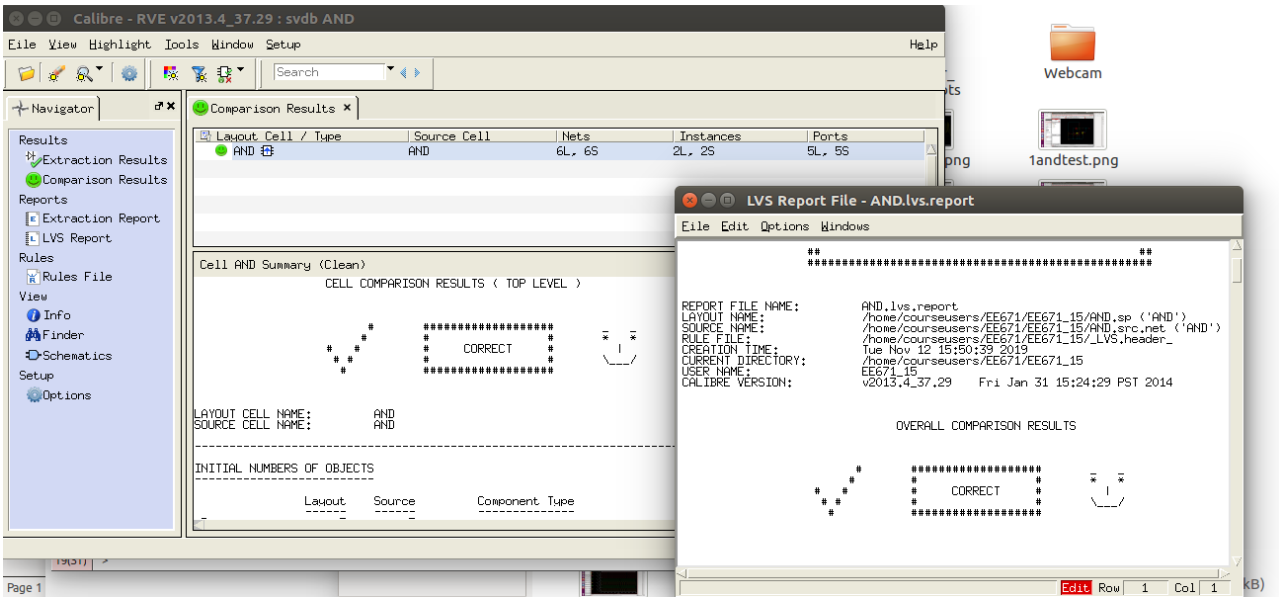

Figure 20: LVS of AND

5.

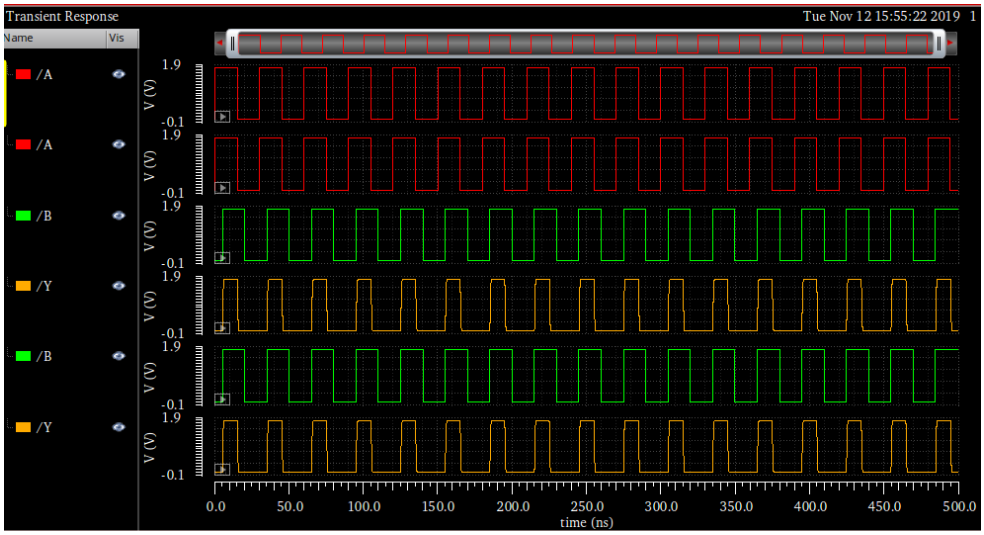

Figure 21: Simulation result of Layout

1.4 $\overline{A+BC}$ gate: (some)

1.

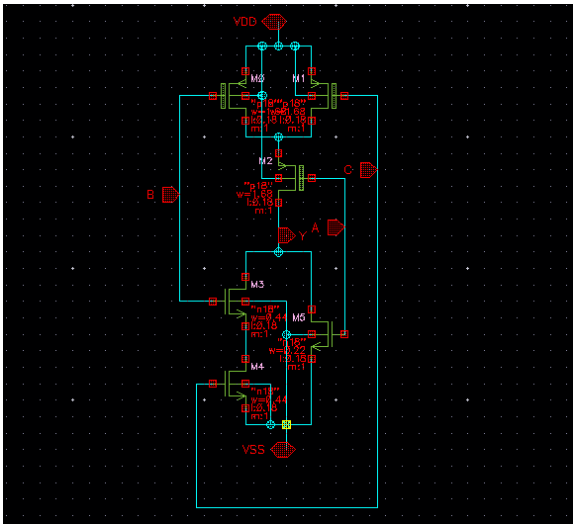

Figure 22: Schematic of some

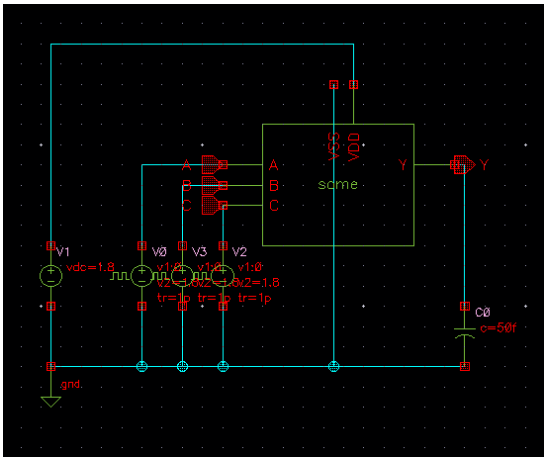

Figure 23: Schematic of some_test

2.

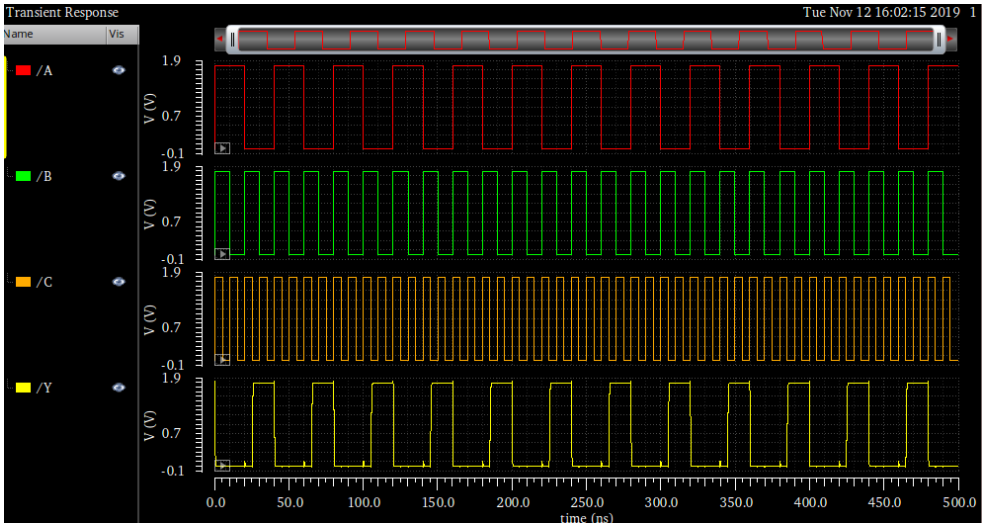

Figure 24: Simulation result of Schematic

3.

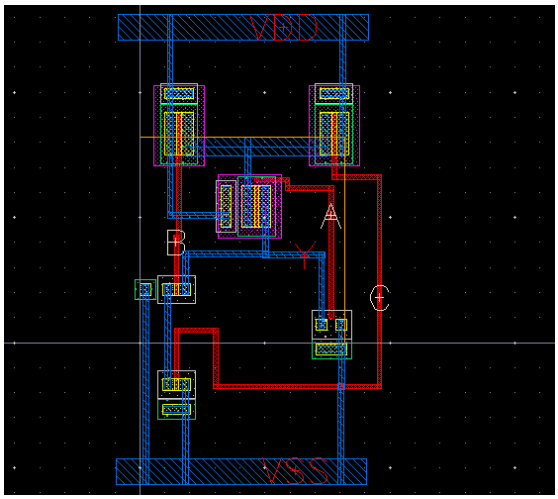

Figure 25: Layout of some

4.

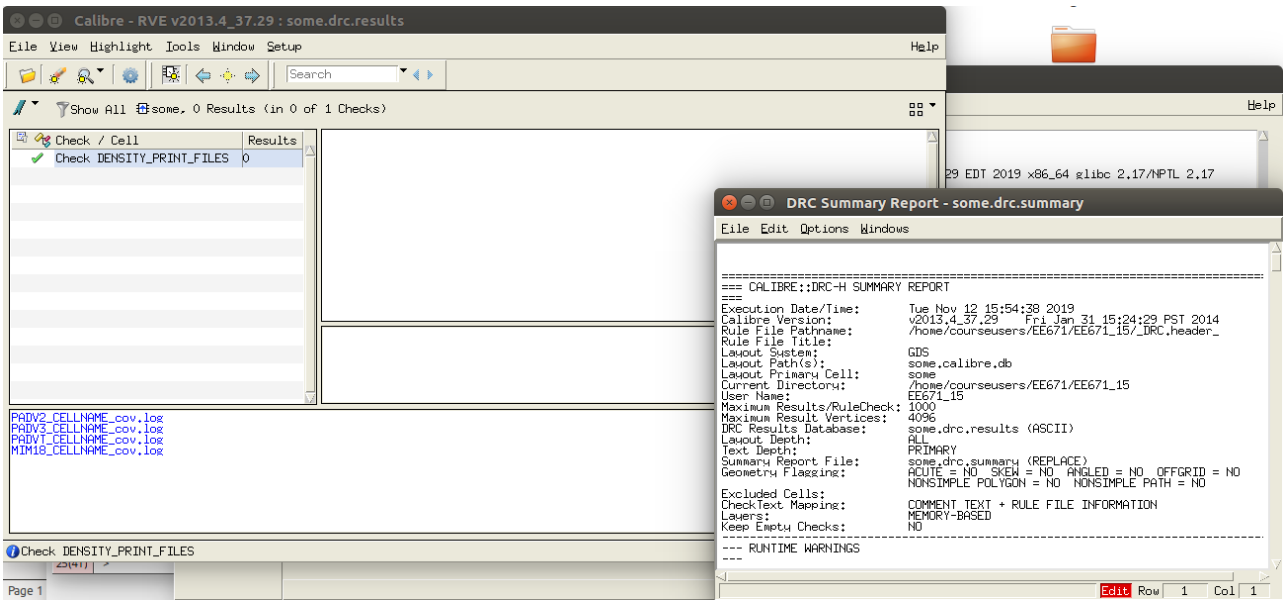

Figure 26: DRC of some

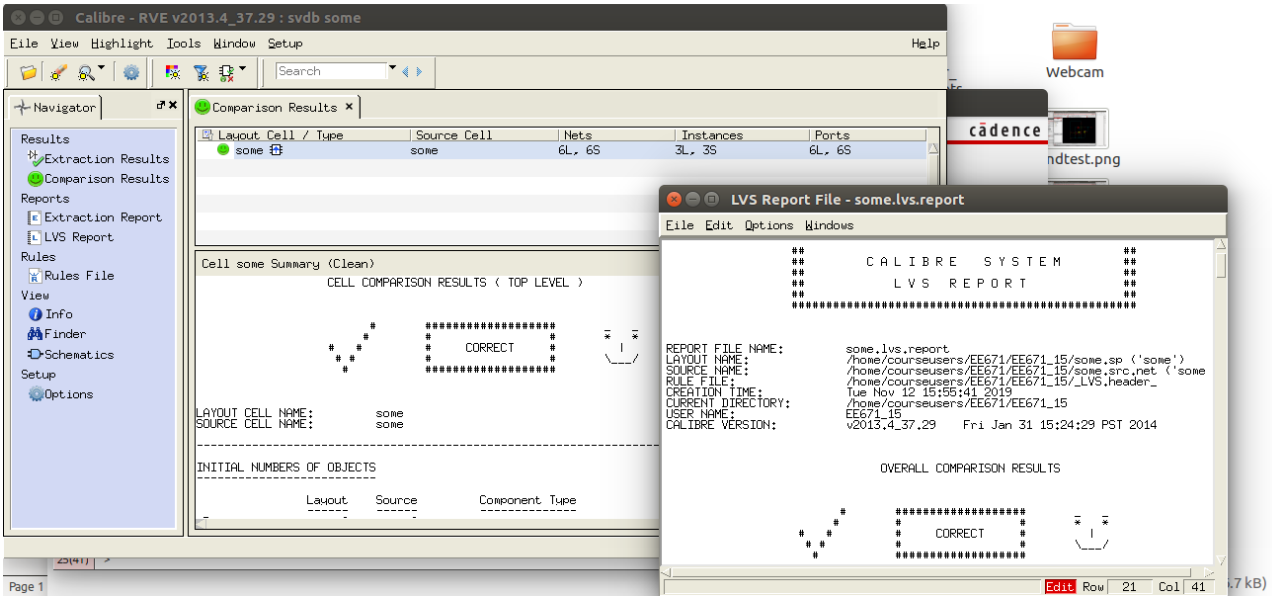

Figure 27: LVS of some

5.

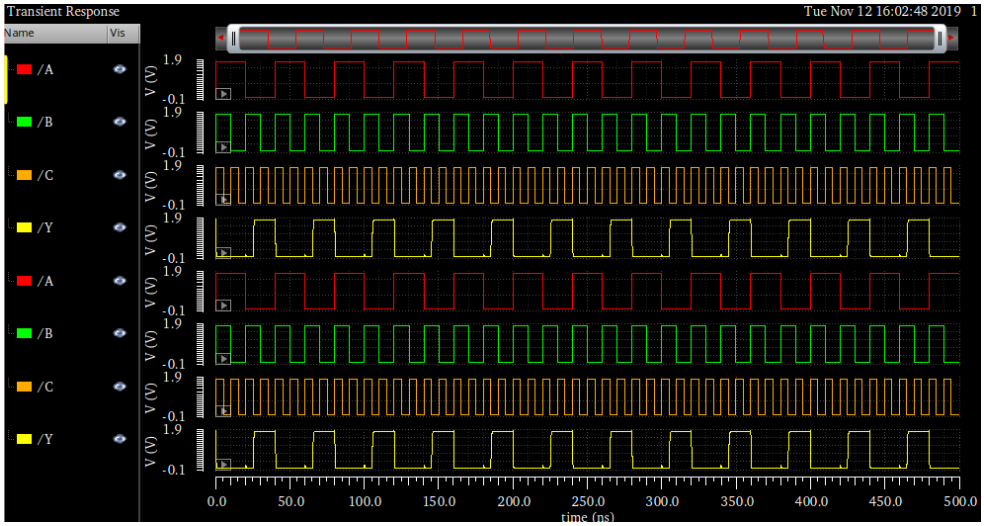

Figure 28: Simulation result of Layout

1.5 $A + BC$ gate: (somen)

1.

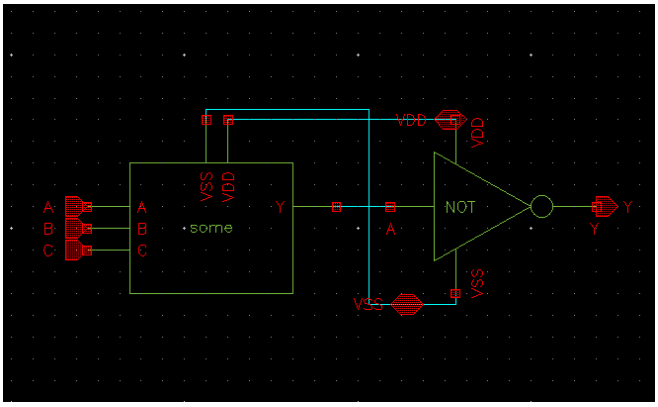

Figure 29: Schematic of somen

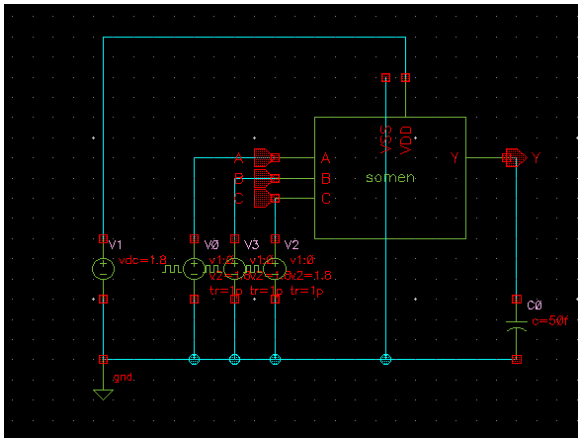

Figure 30: Schematic of somen_test

2.

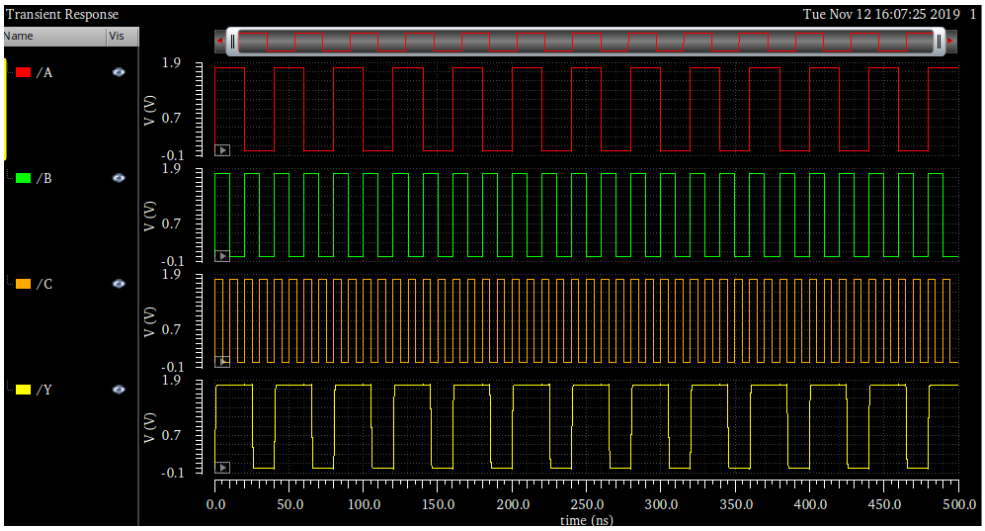

Figure 31: Simulation result of Schematic

3.

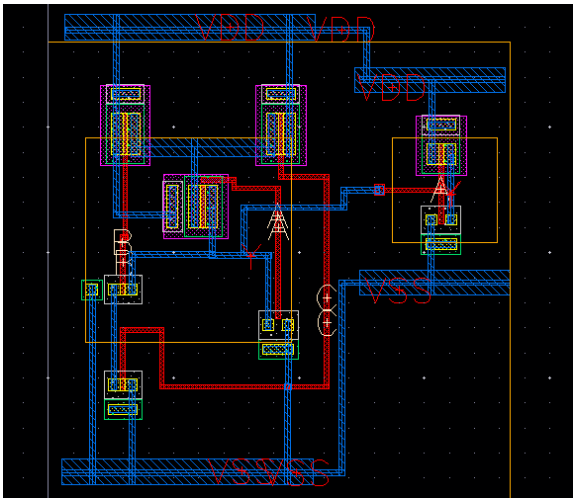

Figure 32: Layout of somen

4.

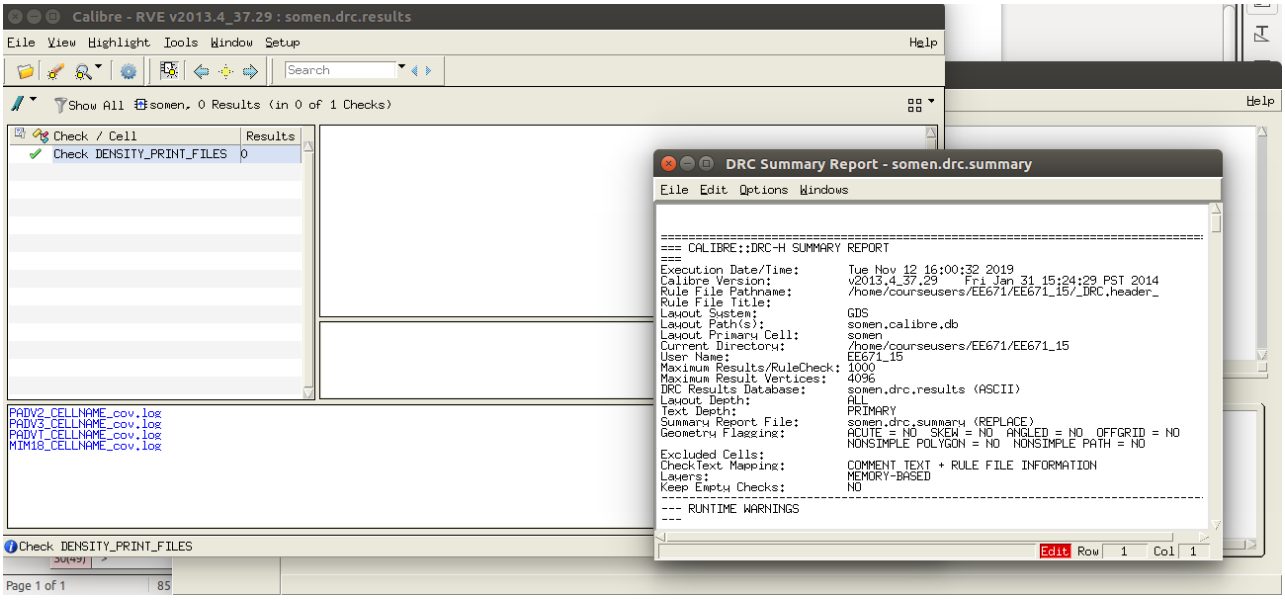

Figure 33: DRC of somen

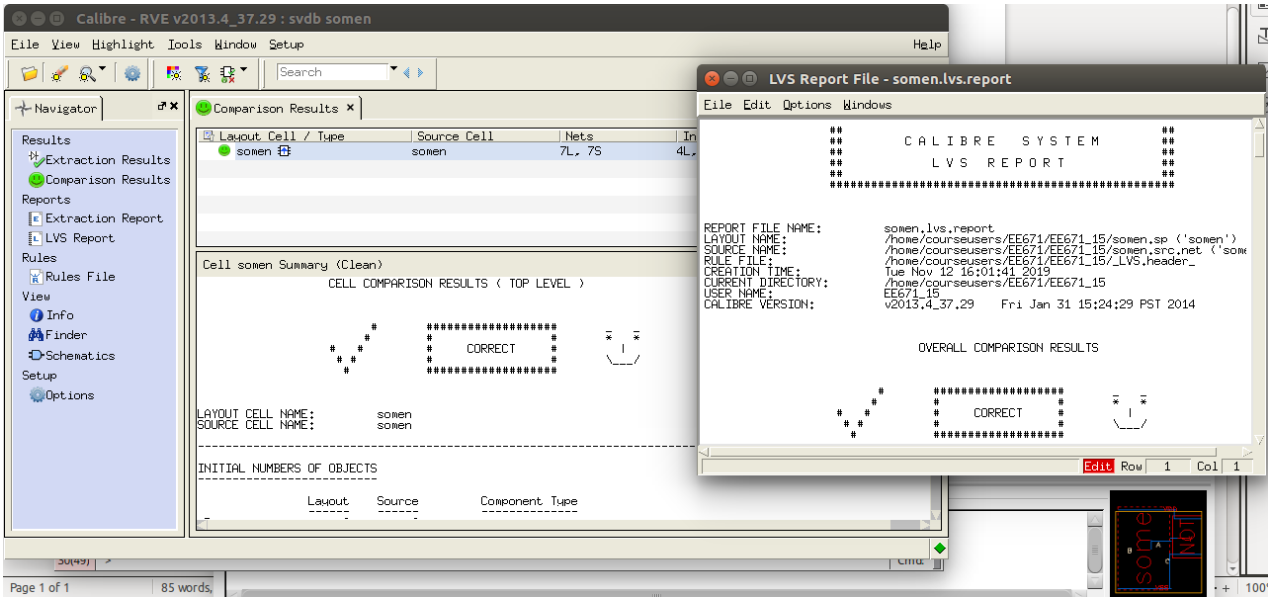

Figure 34: LVS of somen

5.

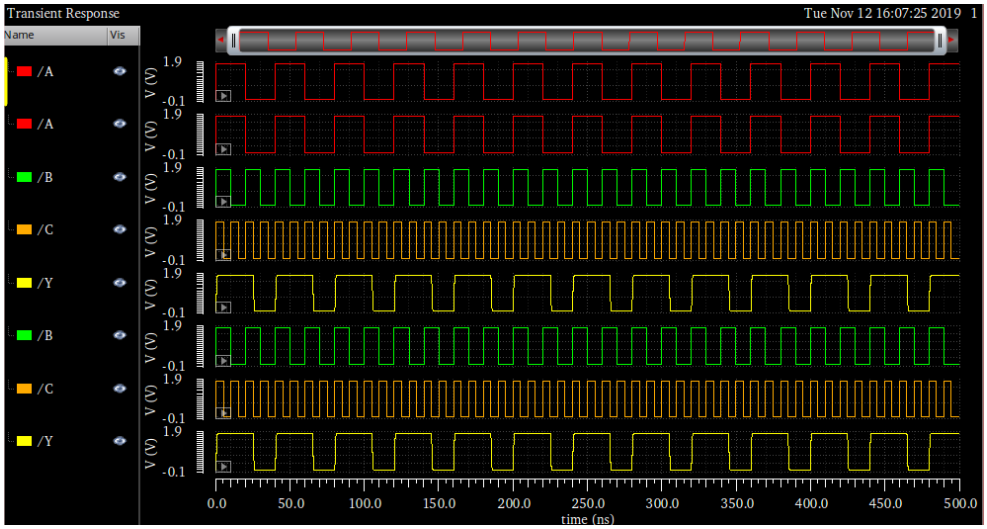

Figure 35: Simulation result of Layout

1.6 Tiny XOR gate: (xor)

1.

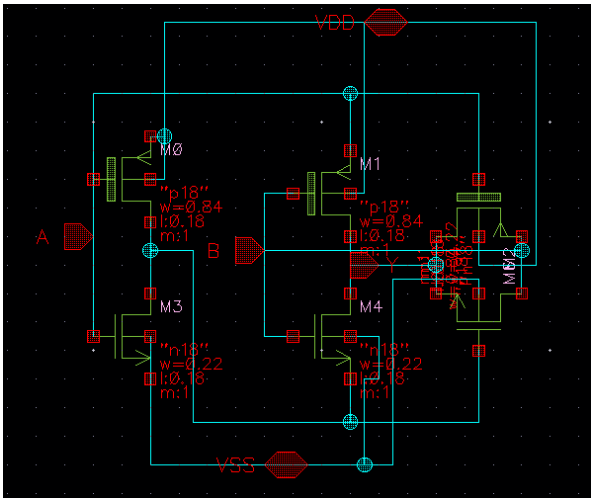

Figure 36: Schematic of xor

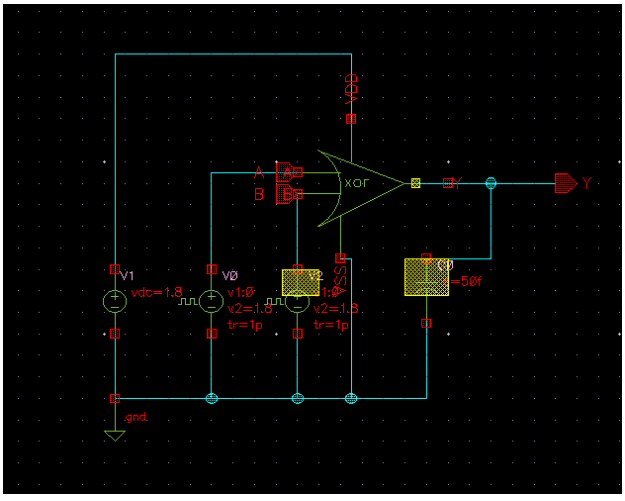

Figure 37: Schematic of xor_test

2.

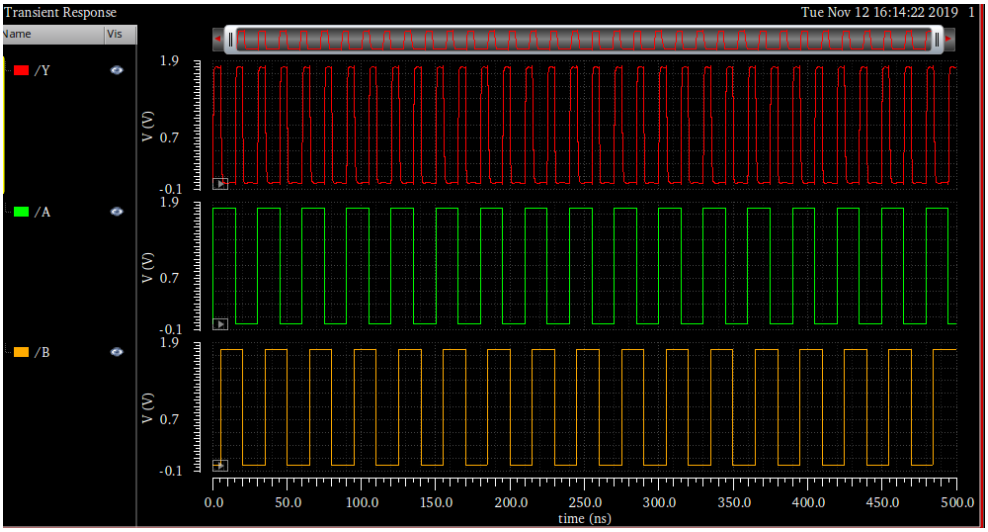

Figure 38: Simulation result of Schematic

3.

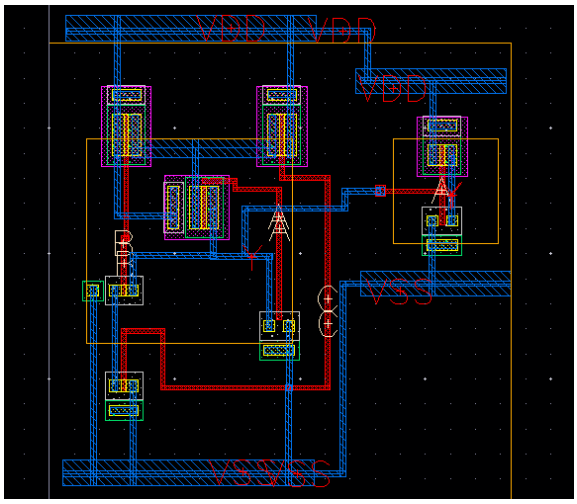

Figure 39: Layout of xor

4.

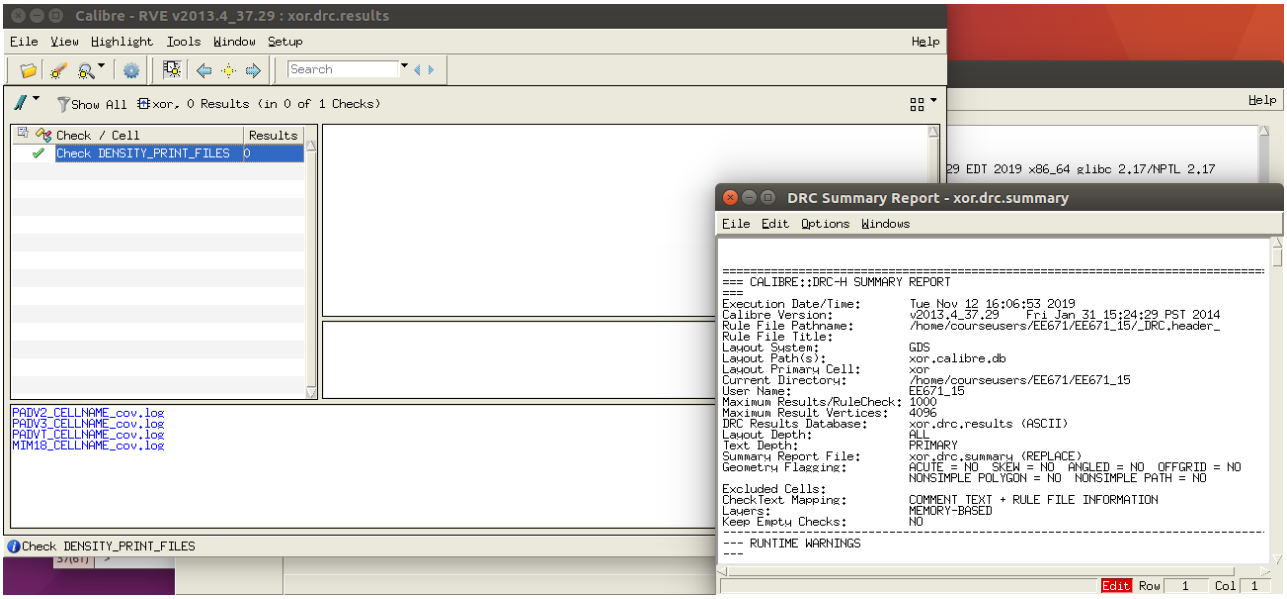

Figure 40: DRC of xor

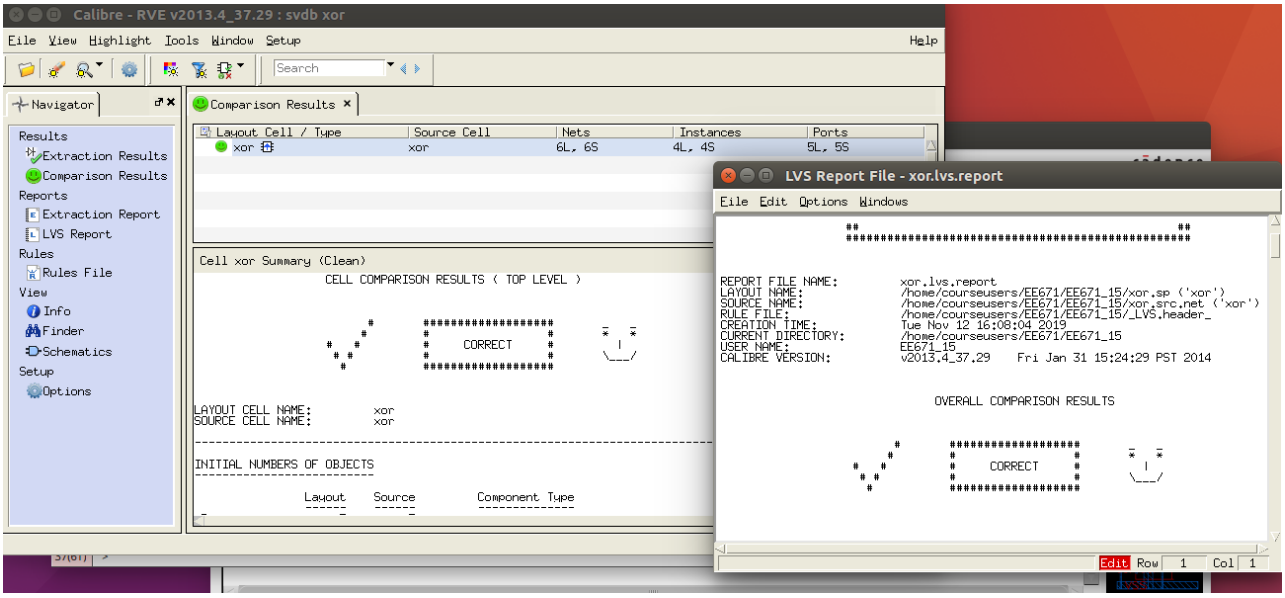

Figure 41: LVS of xor

5.

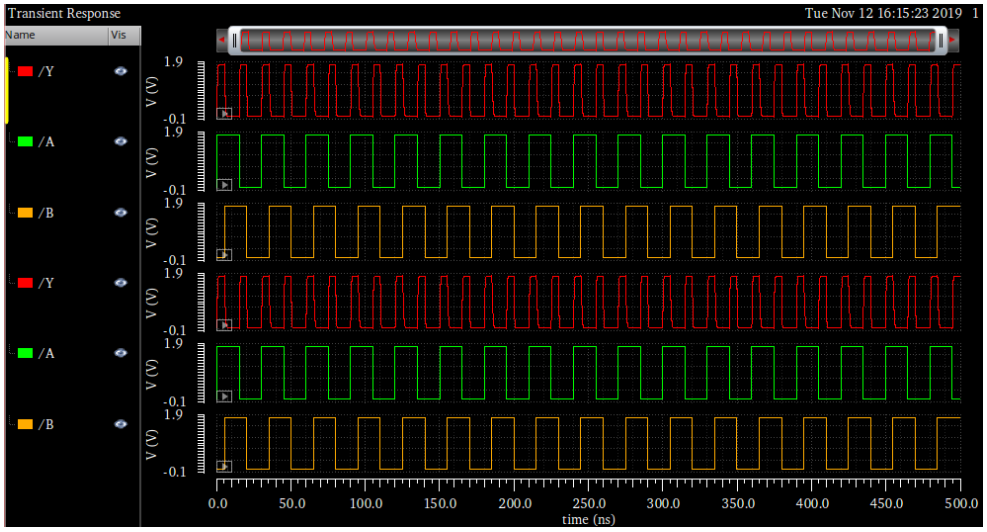

Figure 42: Simulation result of Layout

1.7 Calculating P_i and G_i from inputs: (pg1)

1.

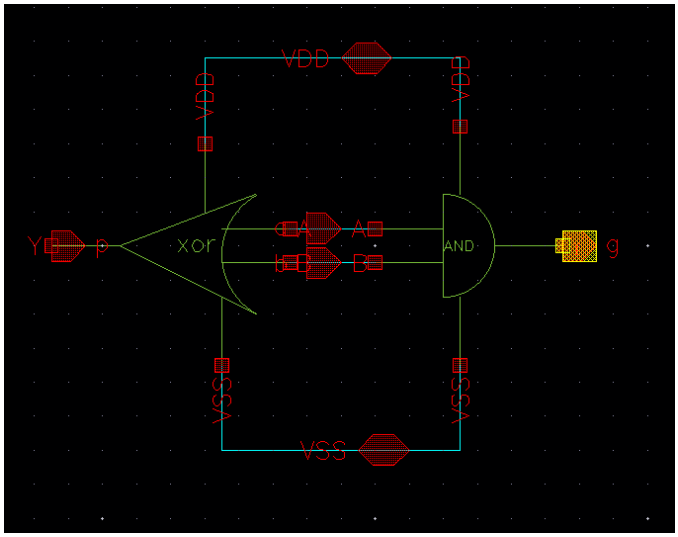

Figure 43: Schematic of pg1

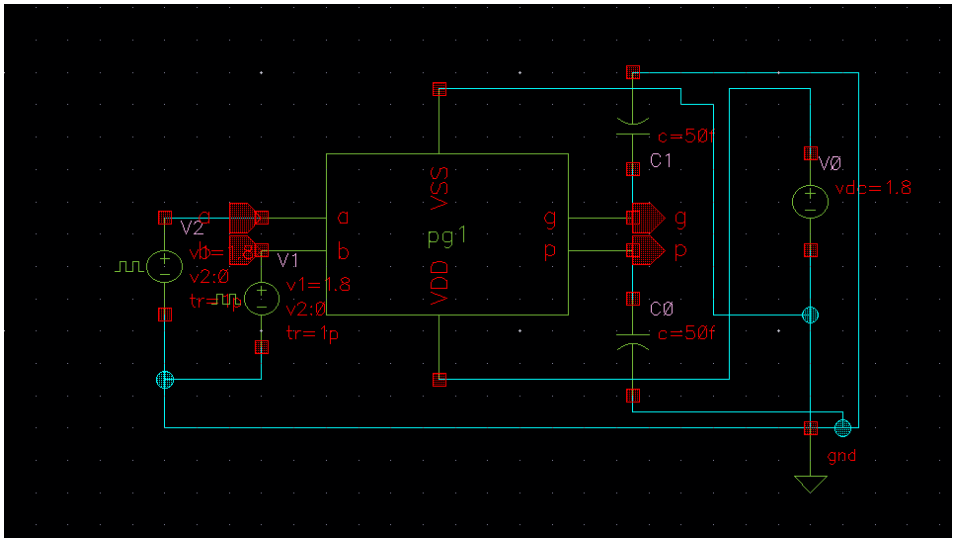

Figure 44: Schematic of pg1_test

2.

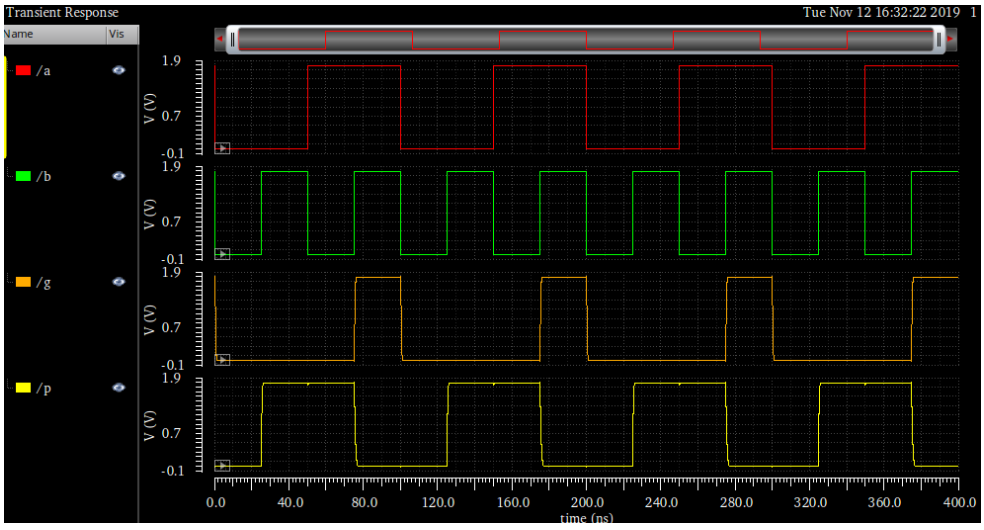

Figure 45: Simulation result of Schematic

3.

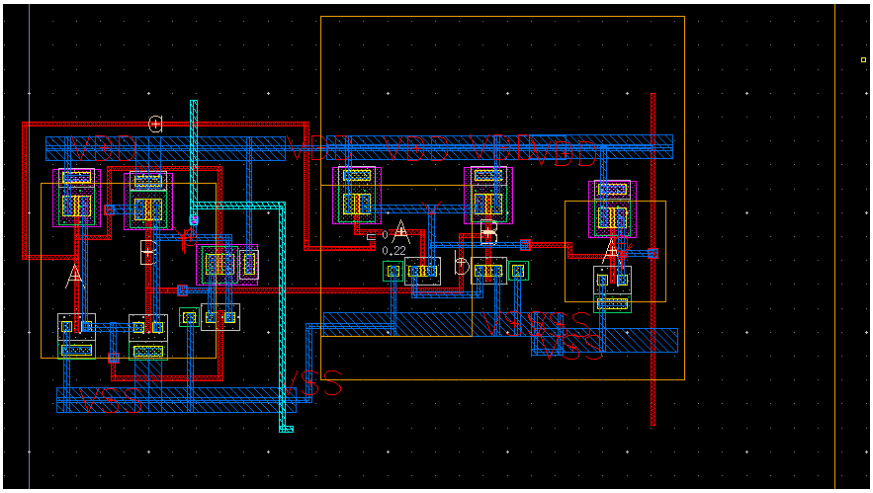

Figure 46: Layout of pg1

4.

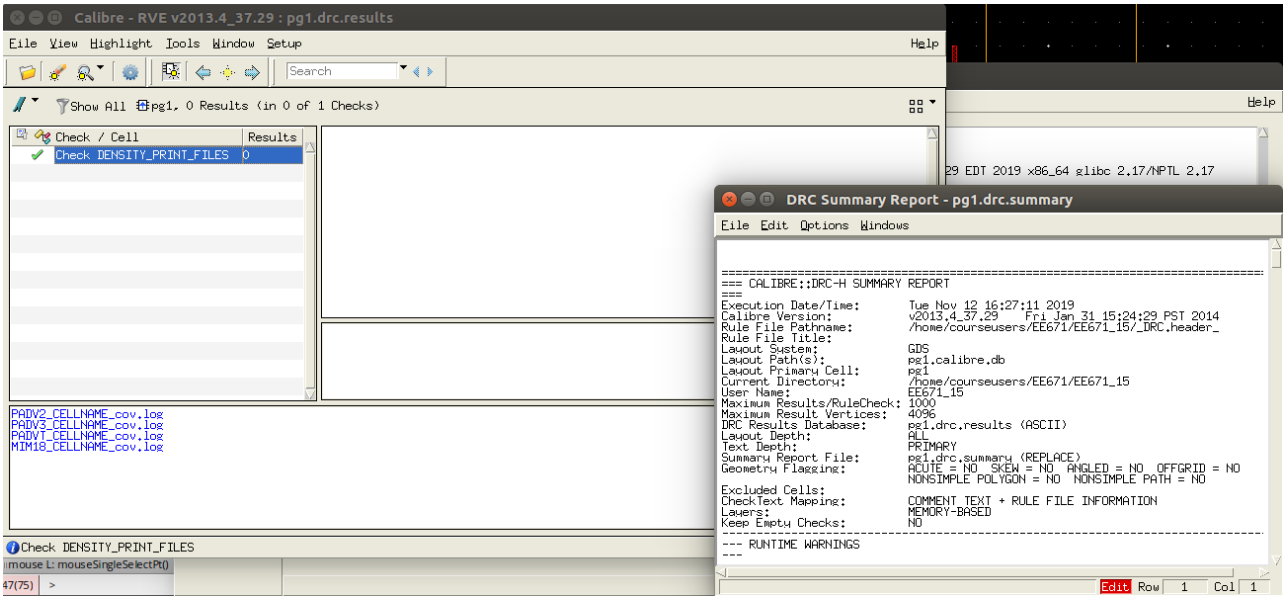

Figure 47: DRC of pg1

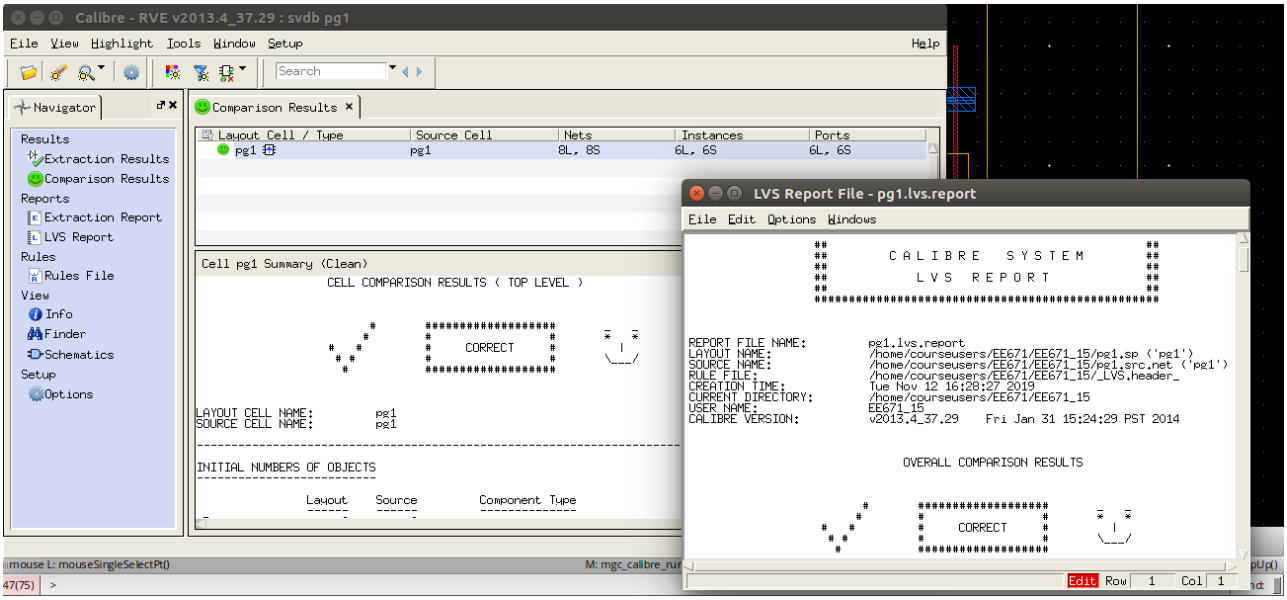

Figure 48: LVS of pg1

5.

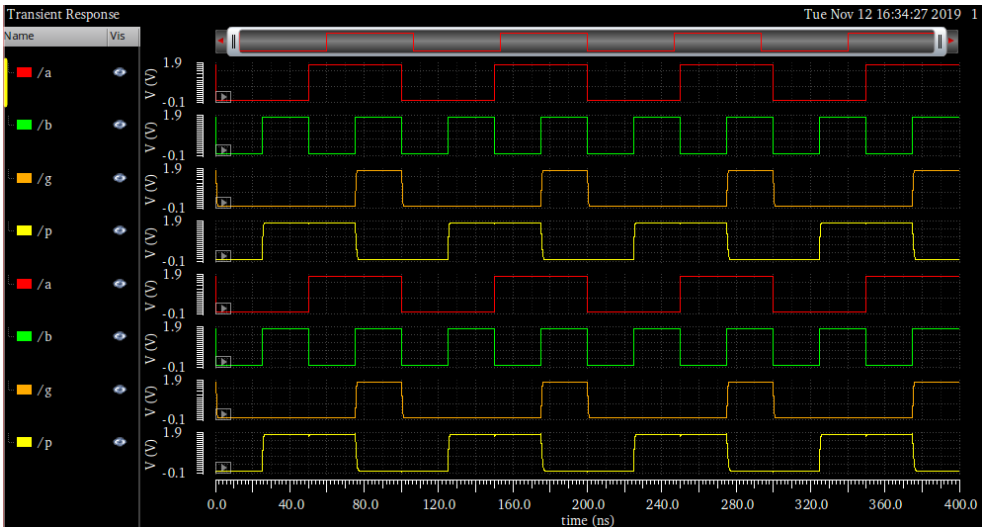

Figure 49: Simulation result of Layout

1.8 Block of 16 pg1: (propgrop1)

1.

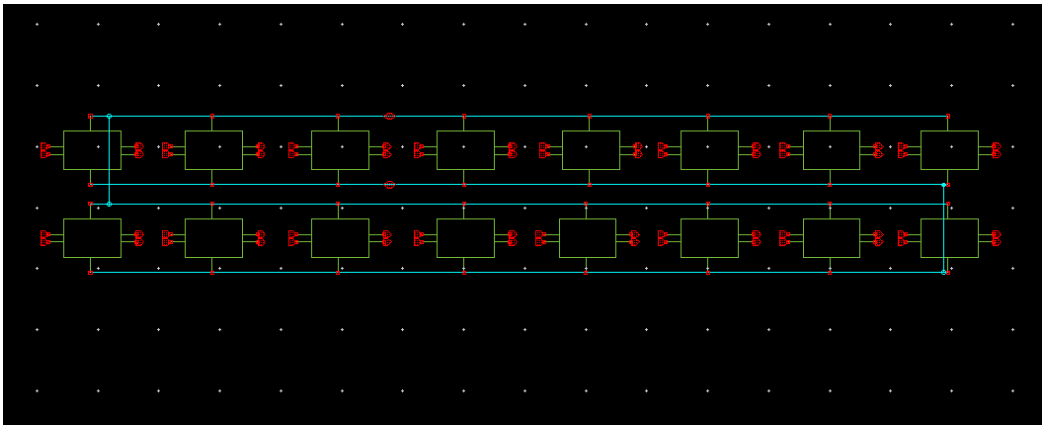

Figure 50: Schematic of propgrop1

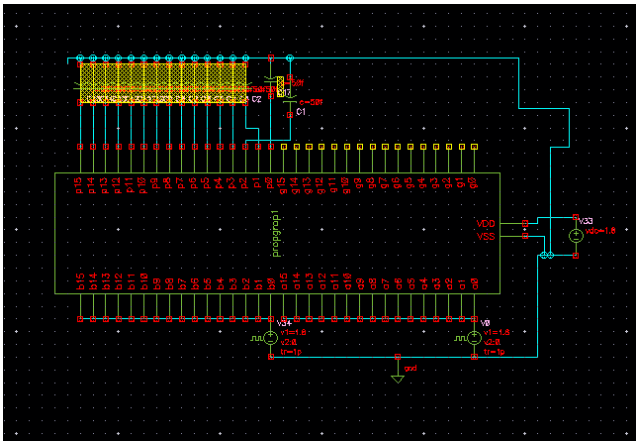

Figure 51: Schematic of propgrop1_test - Propagation

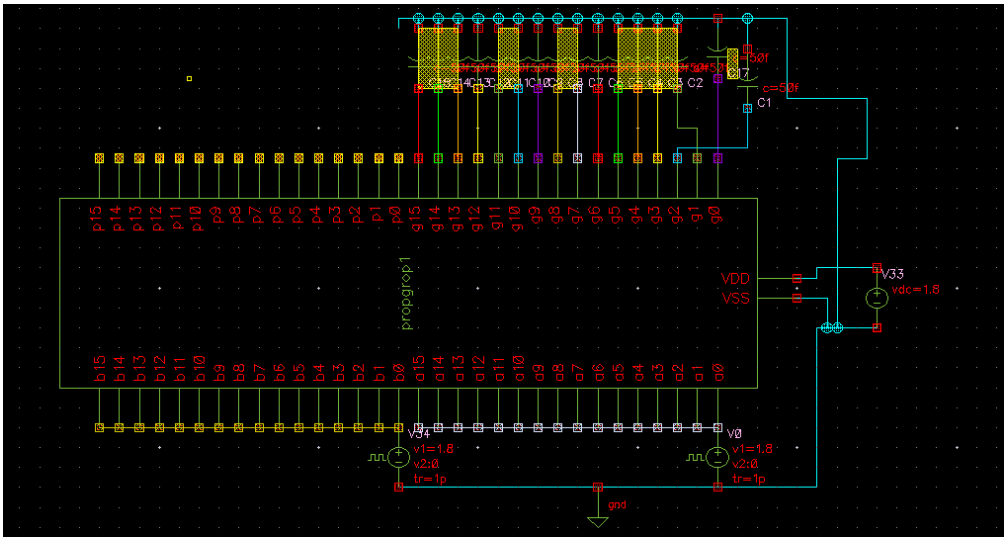

Figure 52: Schematic of propgrop1_test - Generation

2.

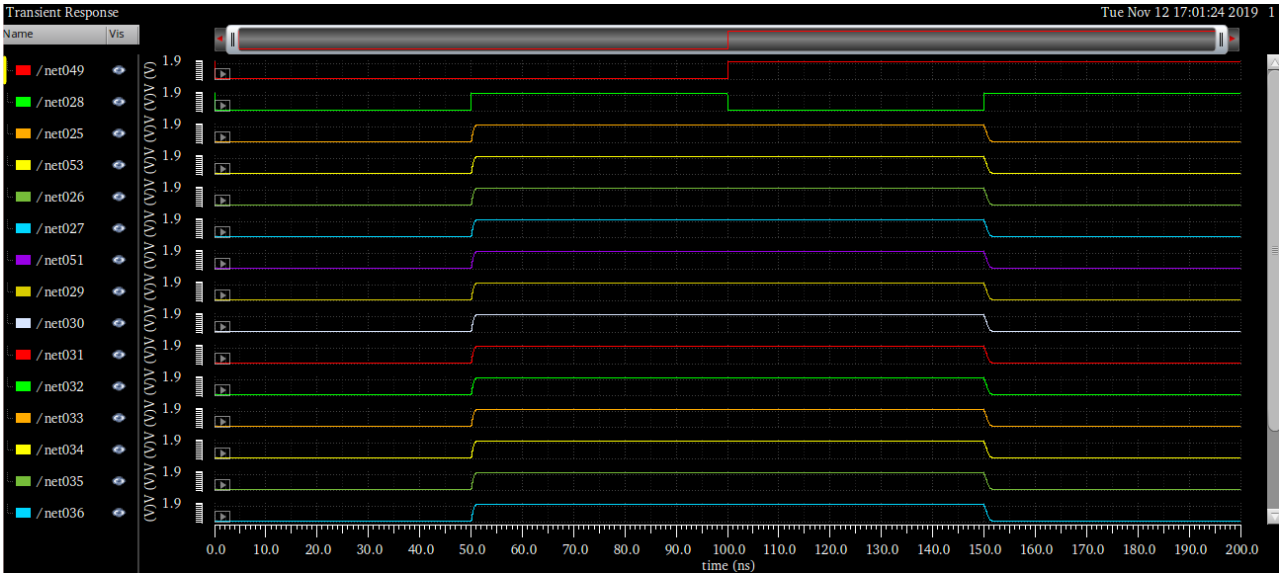

Figure 53: Simulation result of Schematic-Propagation

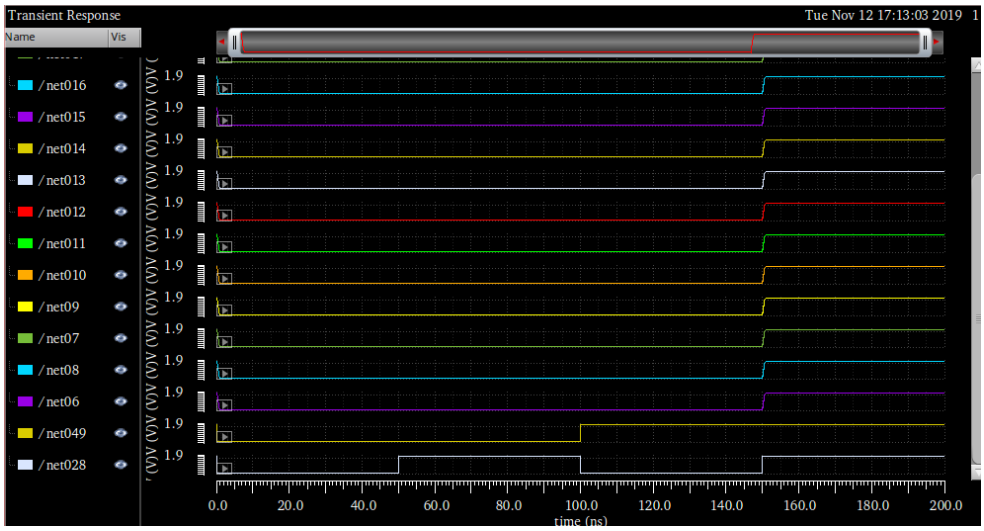

Figure 54: Simulation result of Schematic-Generation

3.

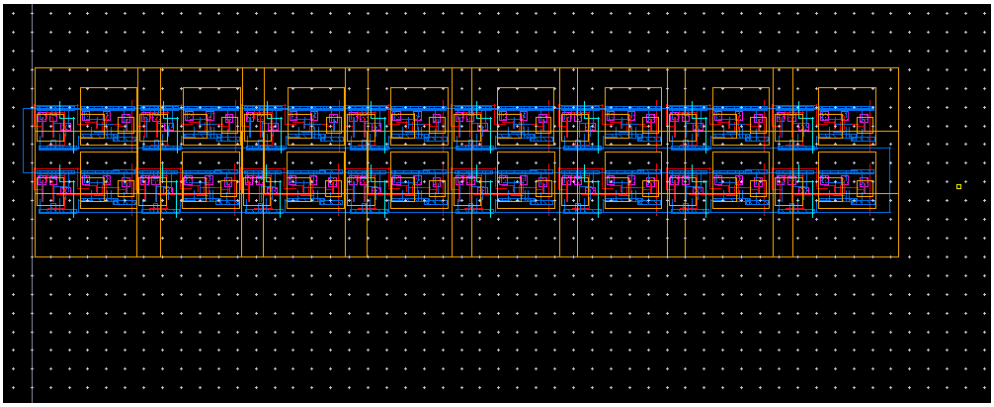

Figure 55: Layout of propgrop1

4.

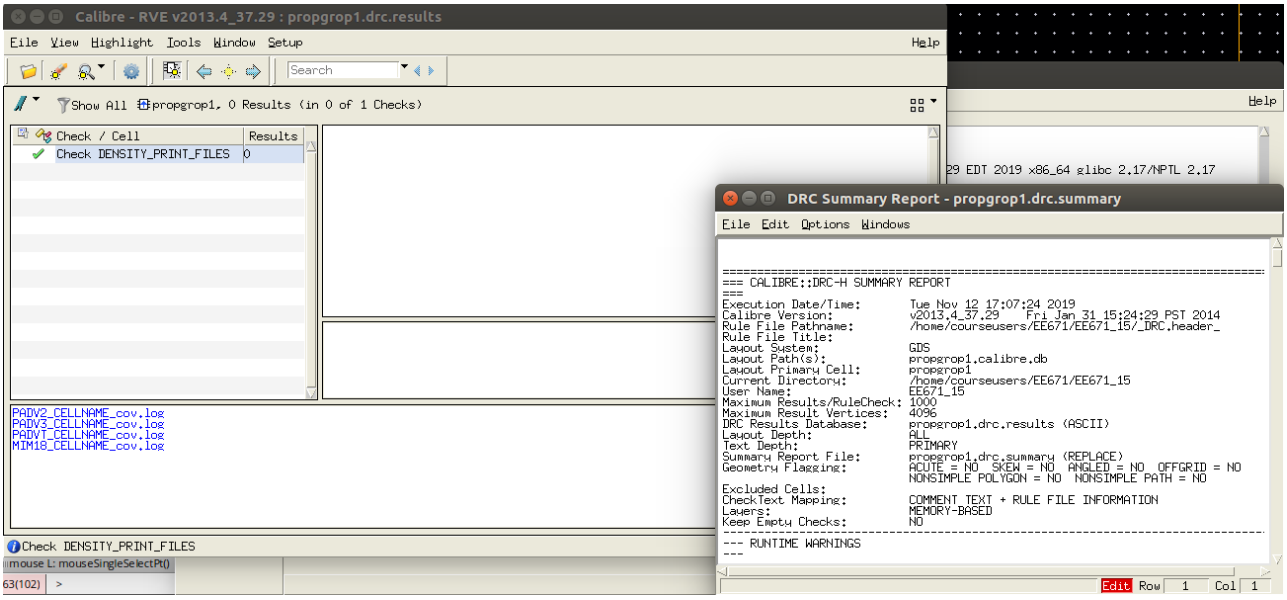

Figure 56: DRC of propgrop1

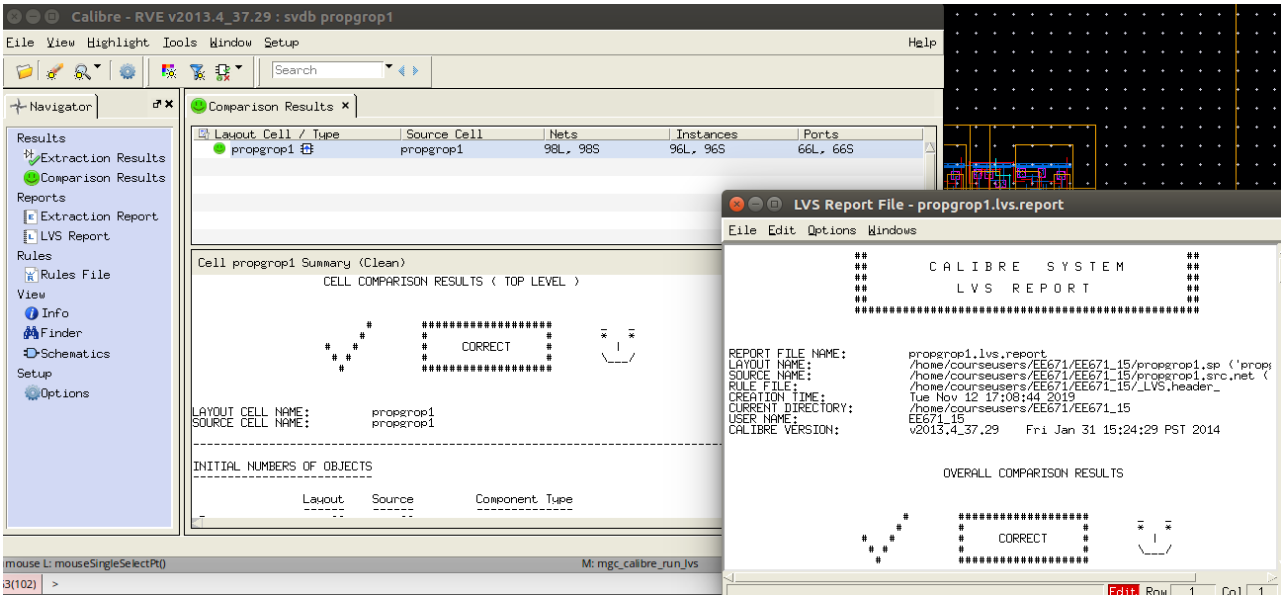

Figure 57: LVS of propgrop1

5.

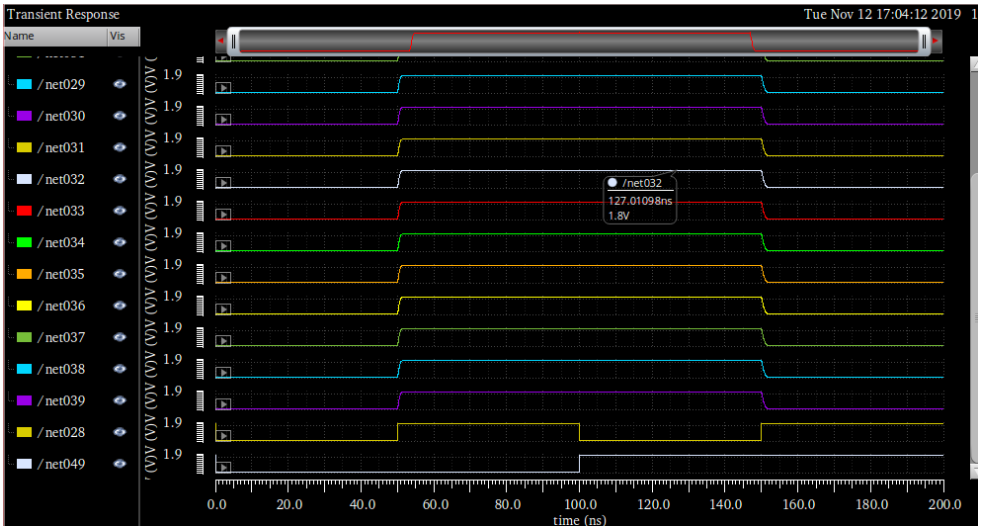

Figure 58: Simulation result of Layout - Propagation

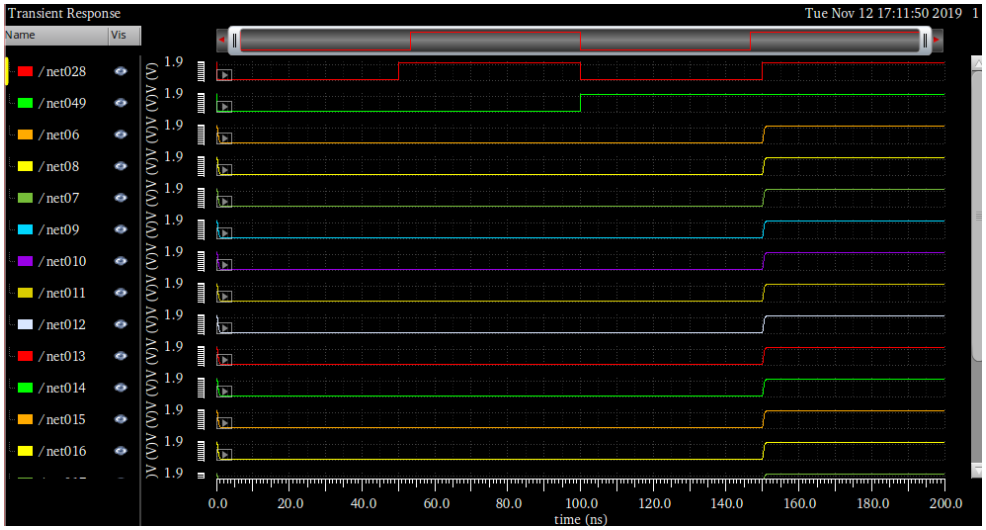

Figure 59: Simulation result of Layout - Generation

1.9 Next P and G Calculator from $P_i, G_i, P_{i-1}, G_{i-1}$: (pg)

1.

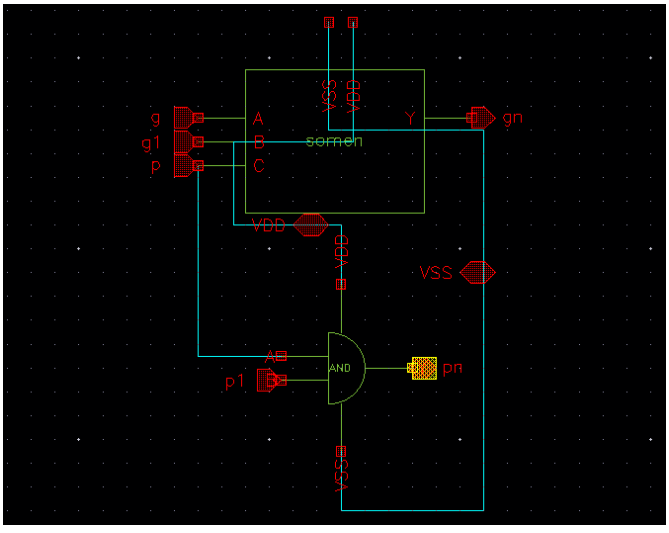

Figure 60: Schematic of pg

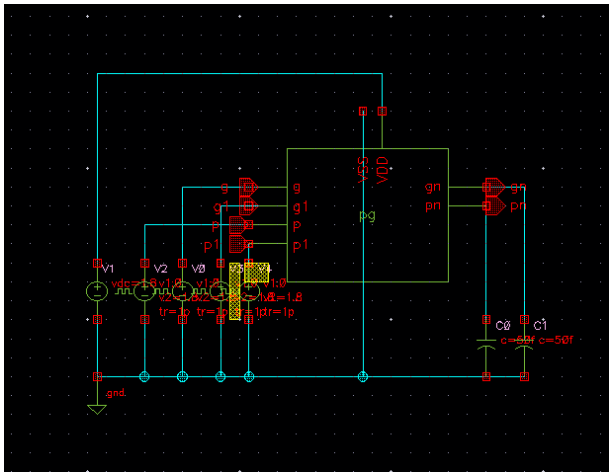

Figure 61: Schematic of pg_test

2.

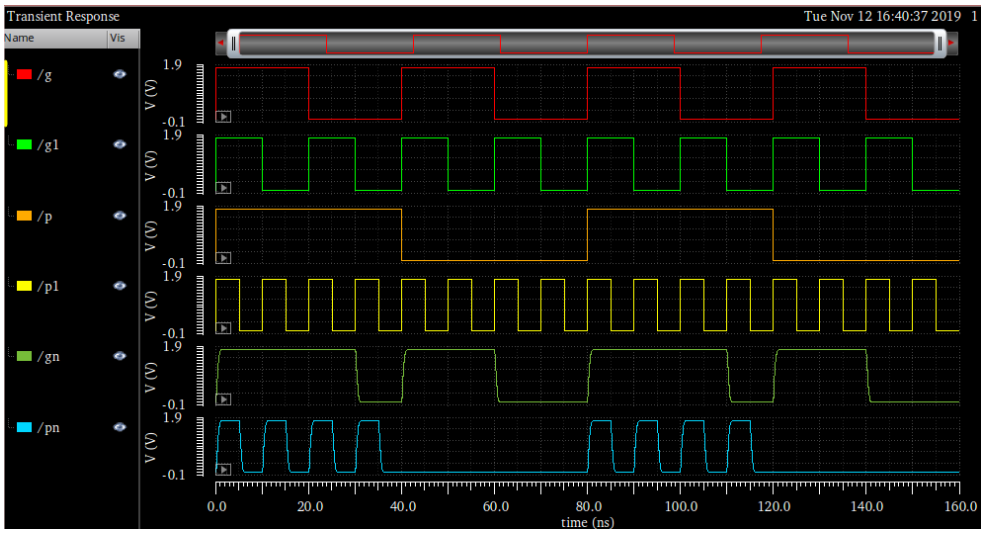

Figure 62: Simulation result of Schematic

3.

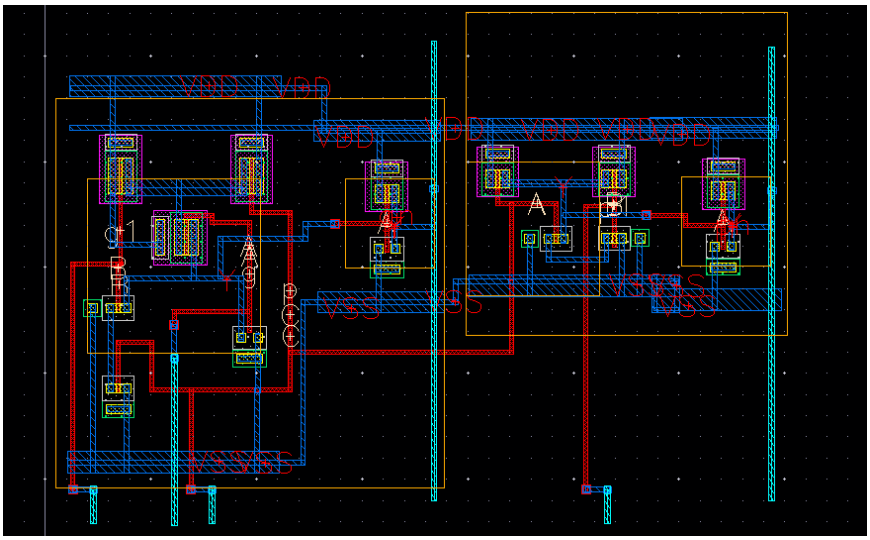

Figure 63: Layout of pg

4.

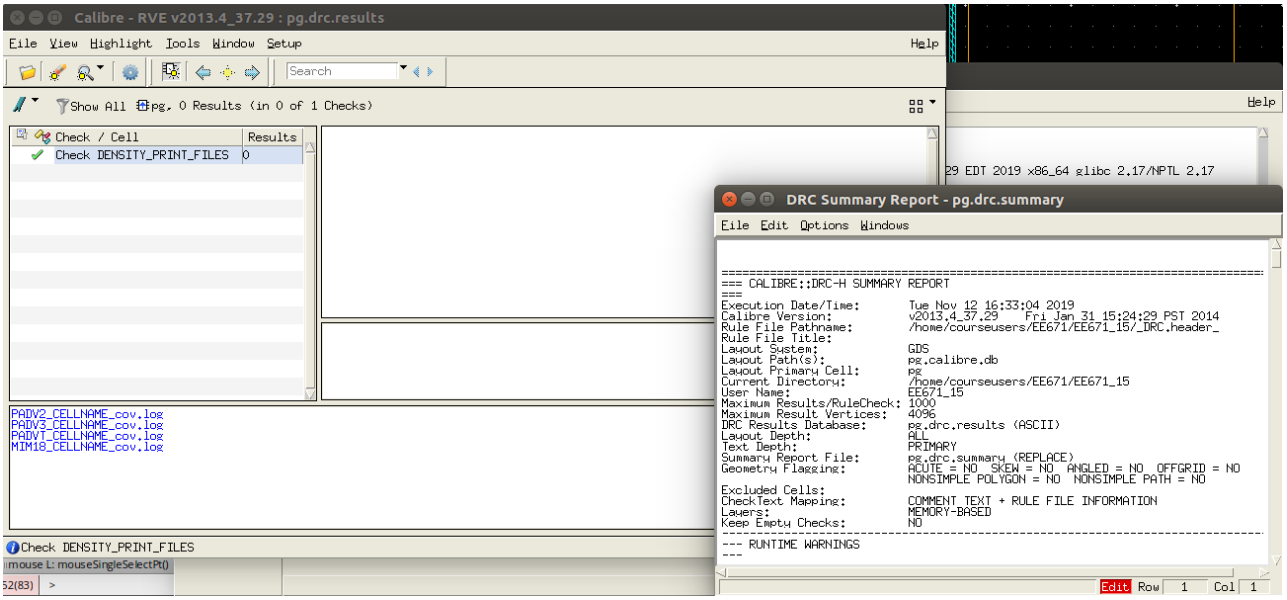

Figure 64: DRC of pg

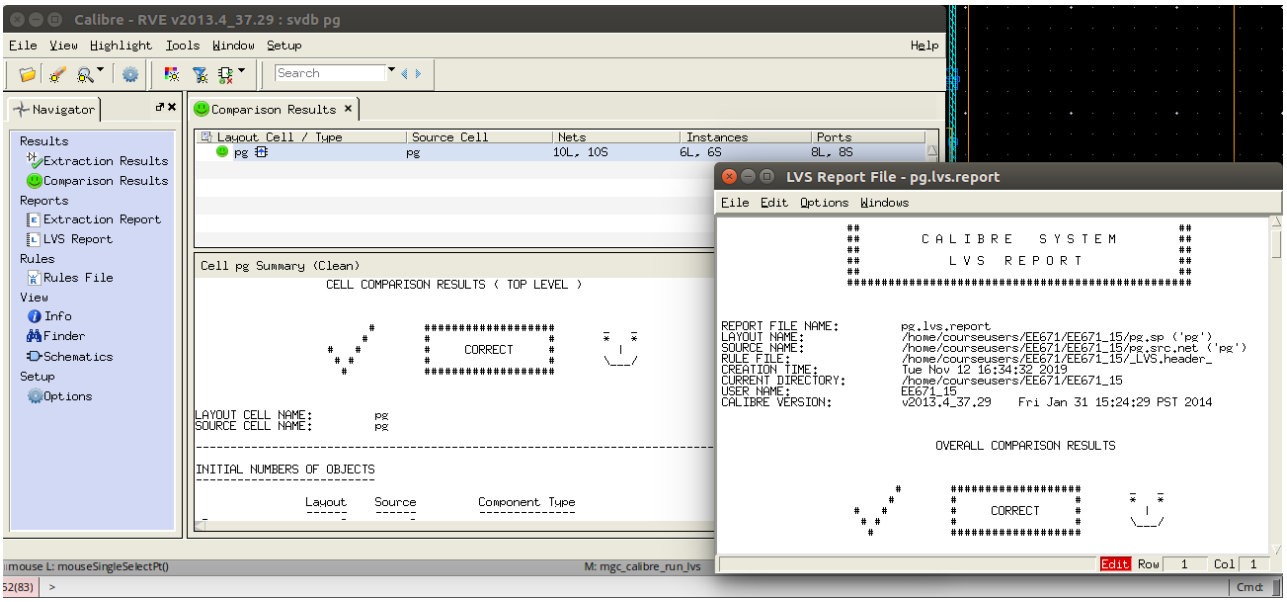

Figure 65: LVS of pg

5.

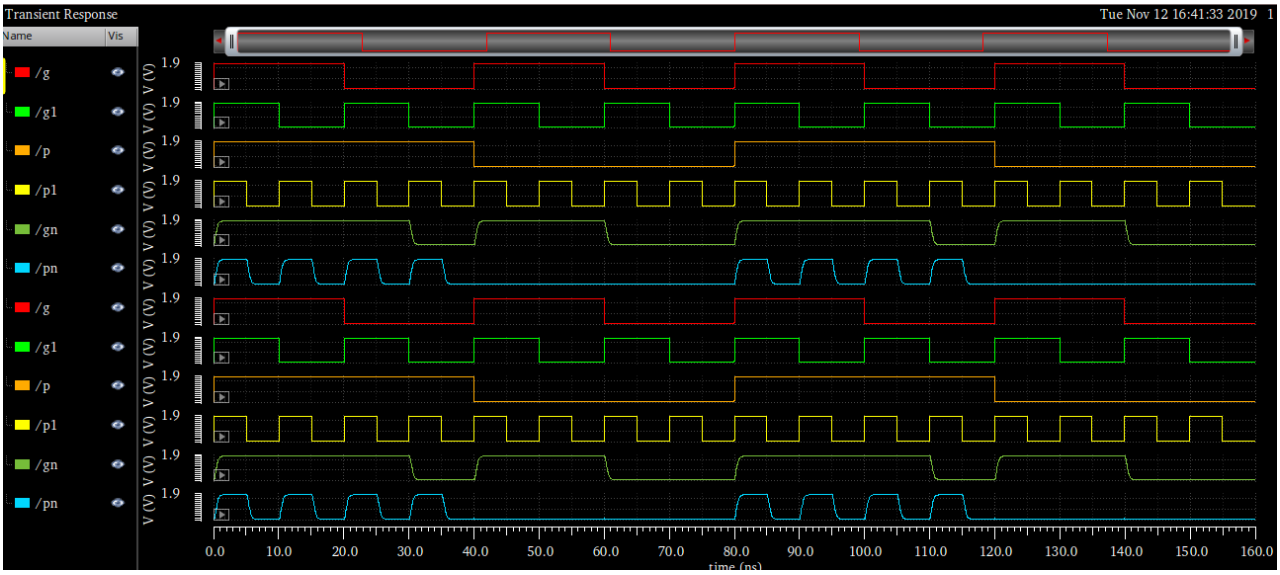

Figure 66: Simulation result of Layout

1.10 16 xor gate set for final sum calculation: (prop)

1.

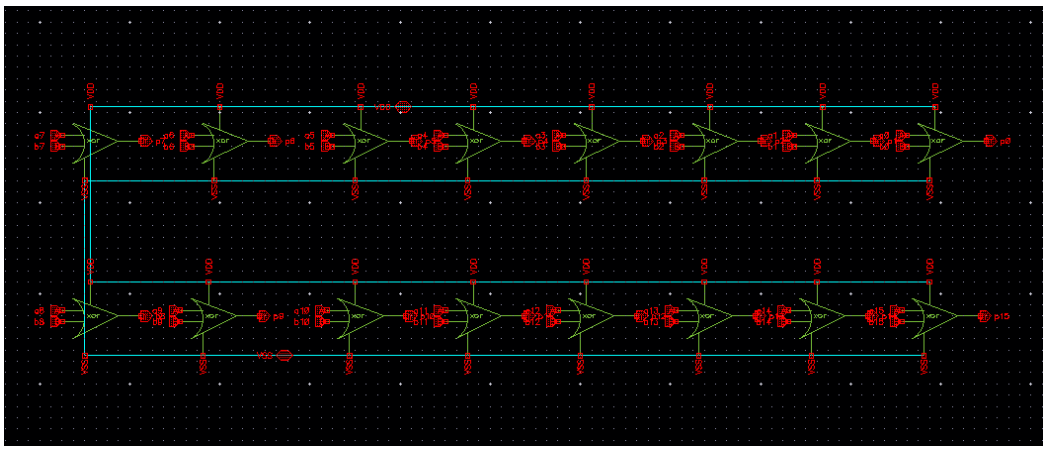

Figure 67: Schematic of prop

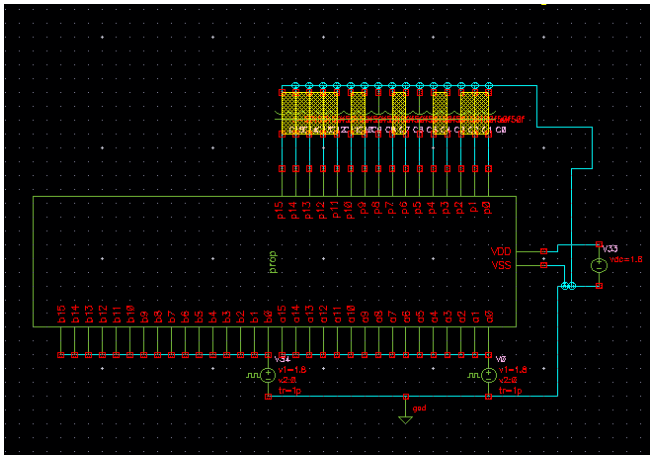

Figure 68: Schematic of prop_test

2.

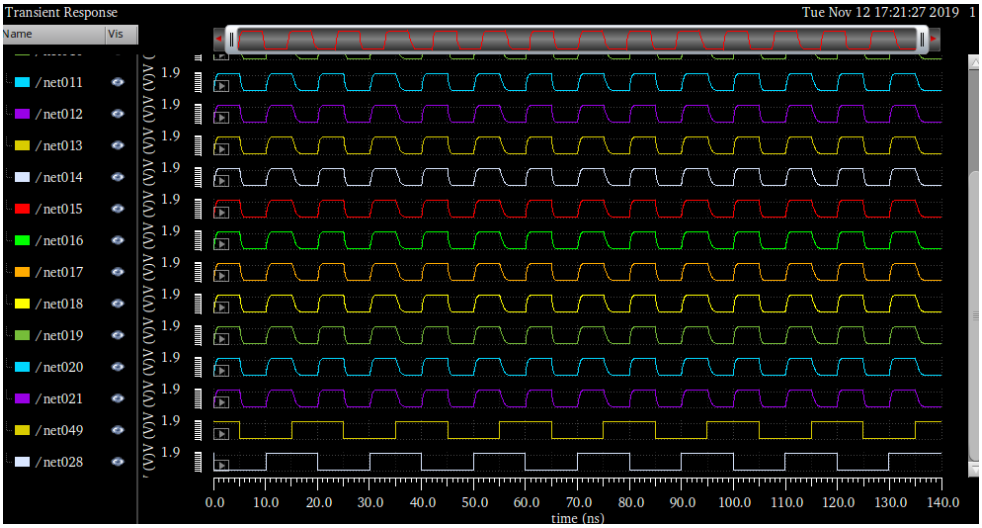

Figure 69: Simulation result of Schematic

3.

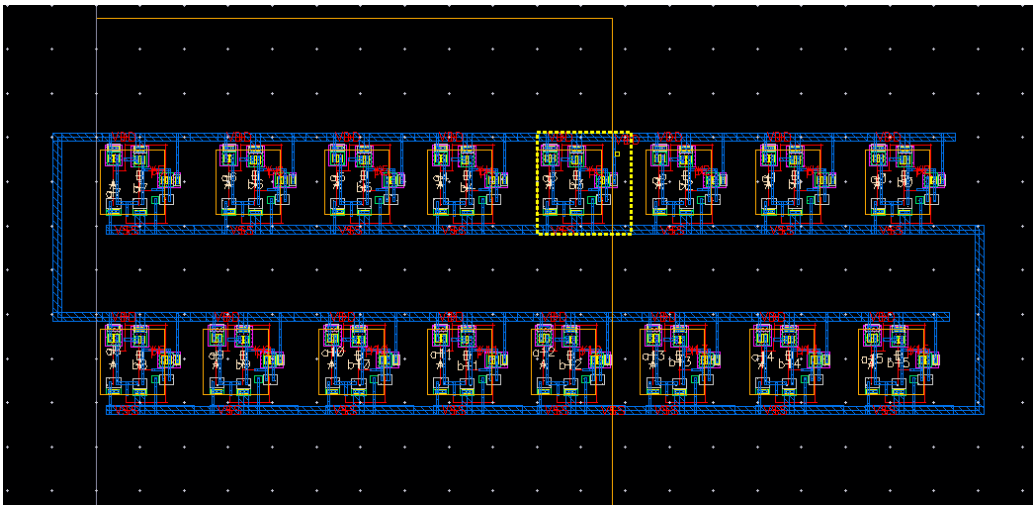

Figure 70: Layout of prop

4.

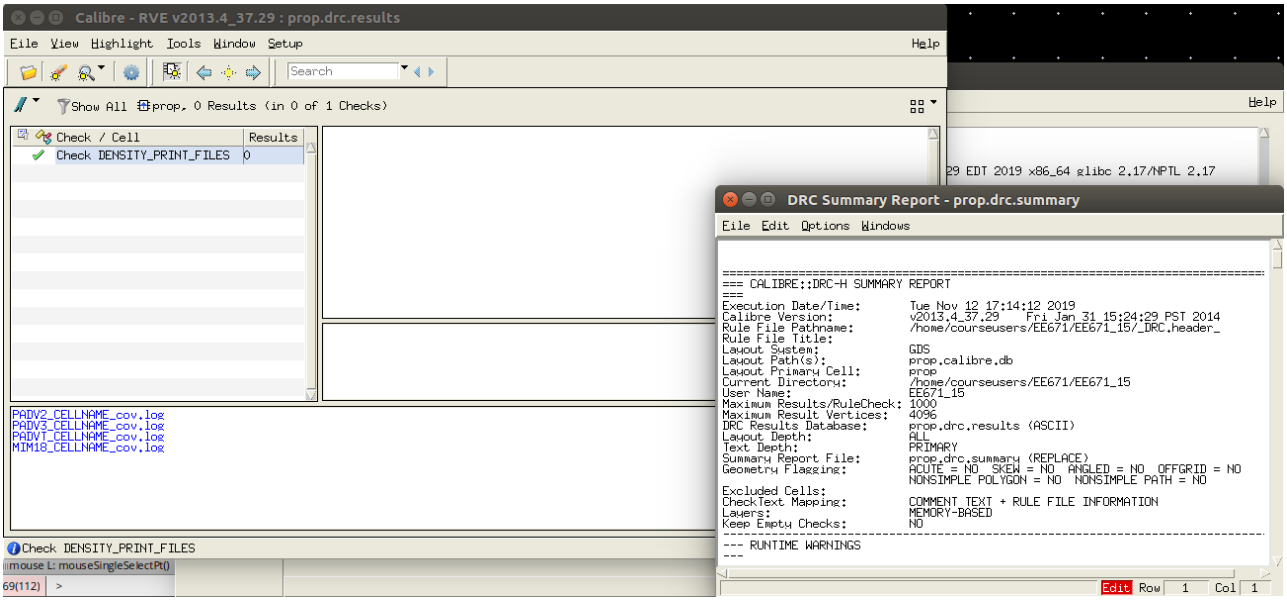

Figure 71: DRC of prop

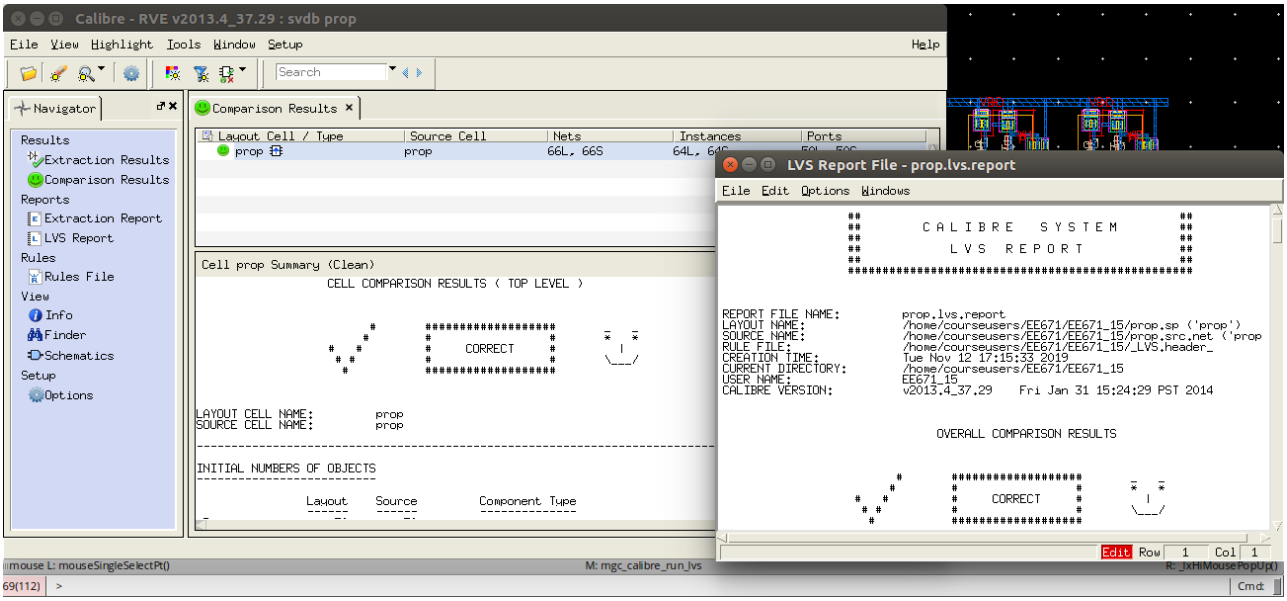

Figure 72: LVS of prop

5.

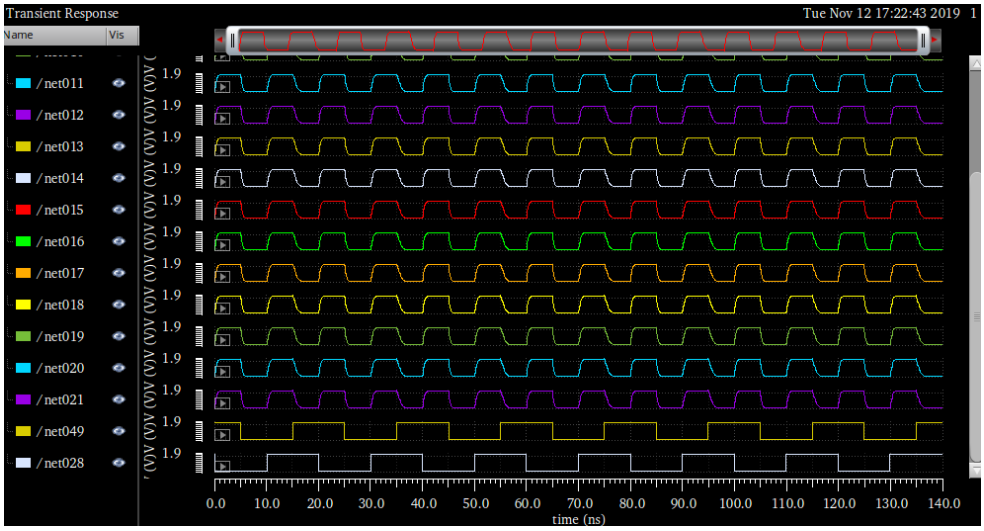

Figure 73: Simulation result of Layout

1.11 Adder: (adder)

1.

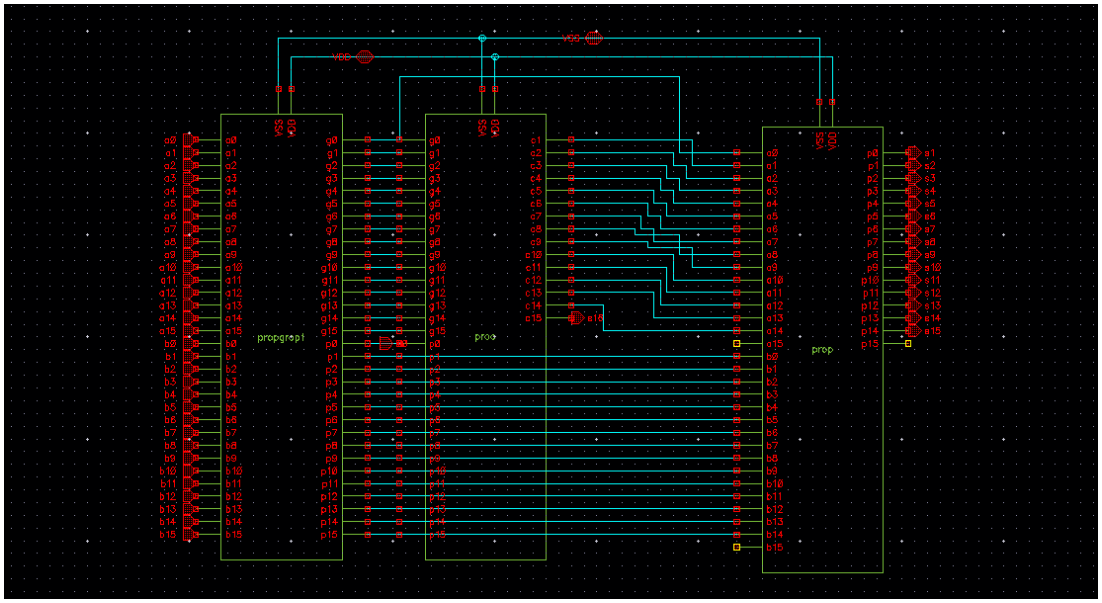

Figure 74: Schematic of adder

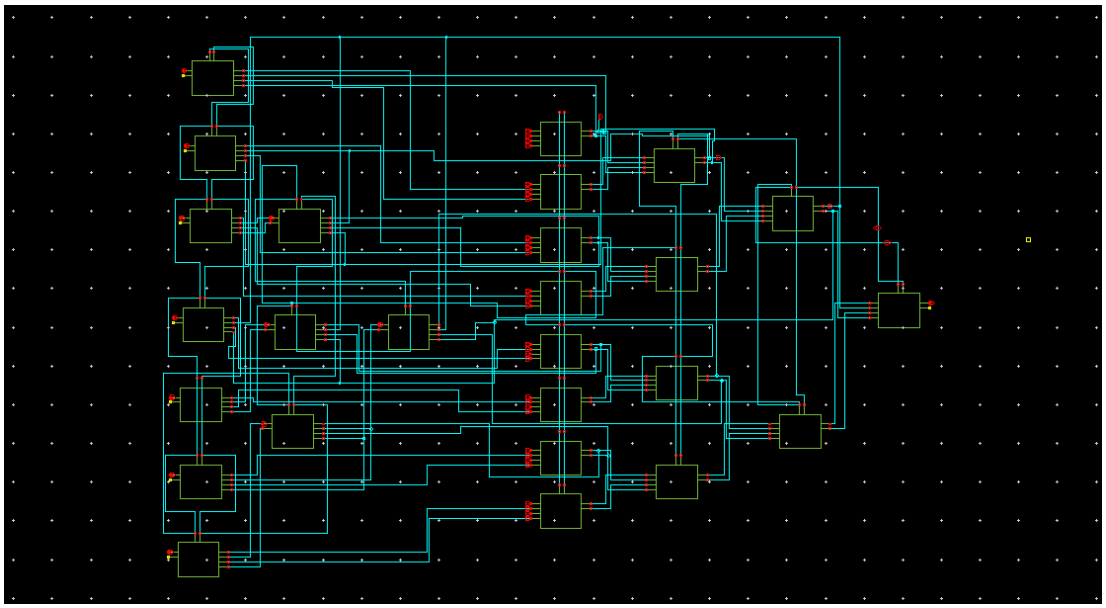

Figure 75: Schematic of proc block of Adder

We have two test adders. First is for the 0-0, 0-65535, 65535-0, 65535-65535 cases and next has alternate bits being 1 and 0.

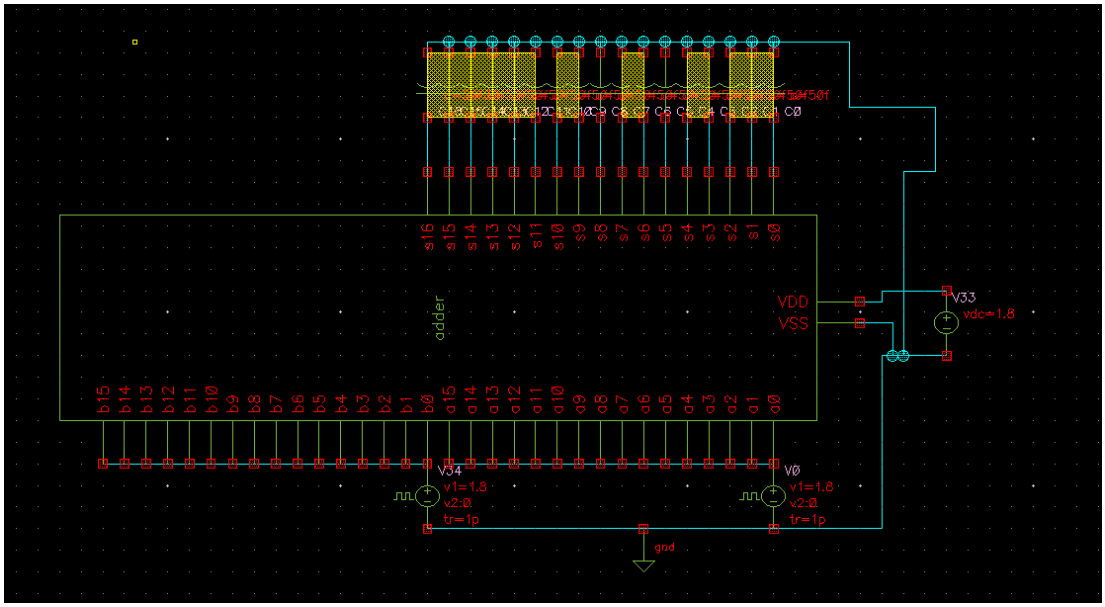

Figure 76: Schematic of first adder_test (adder_test)

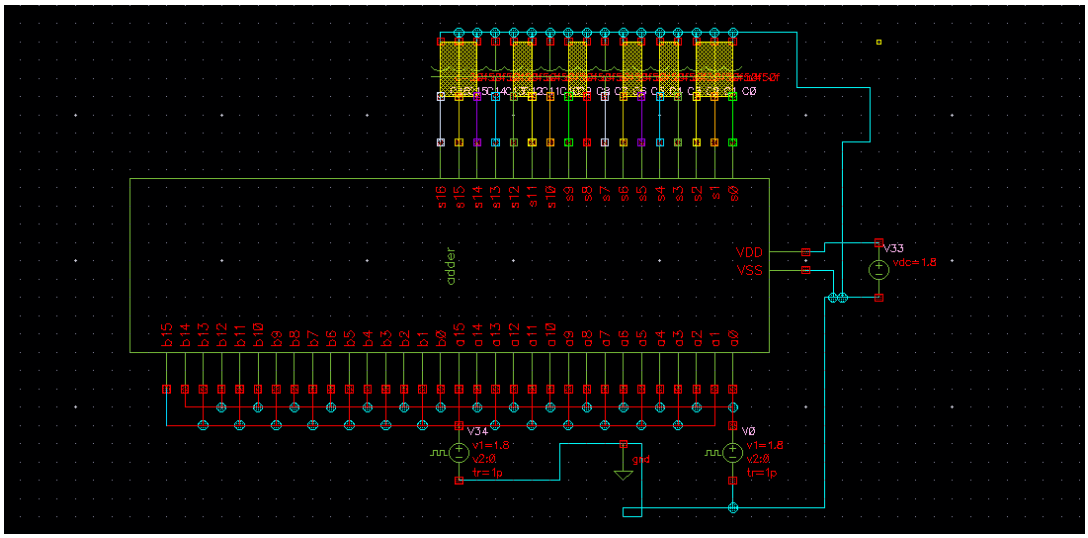

Figure 77: Schematic of second adder_test (adder_test1)

2.

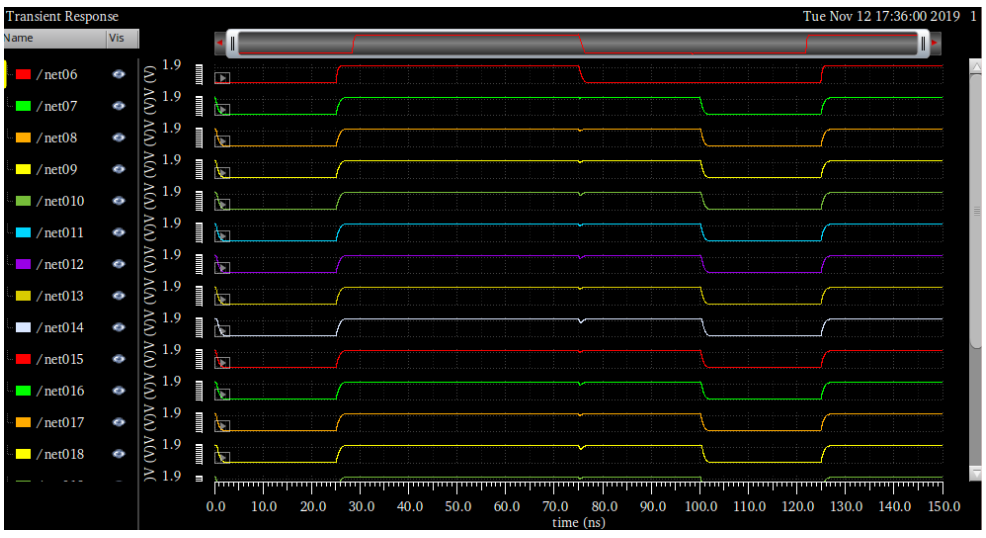

Figure 78: Simulation result of Schematic of first test - 1

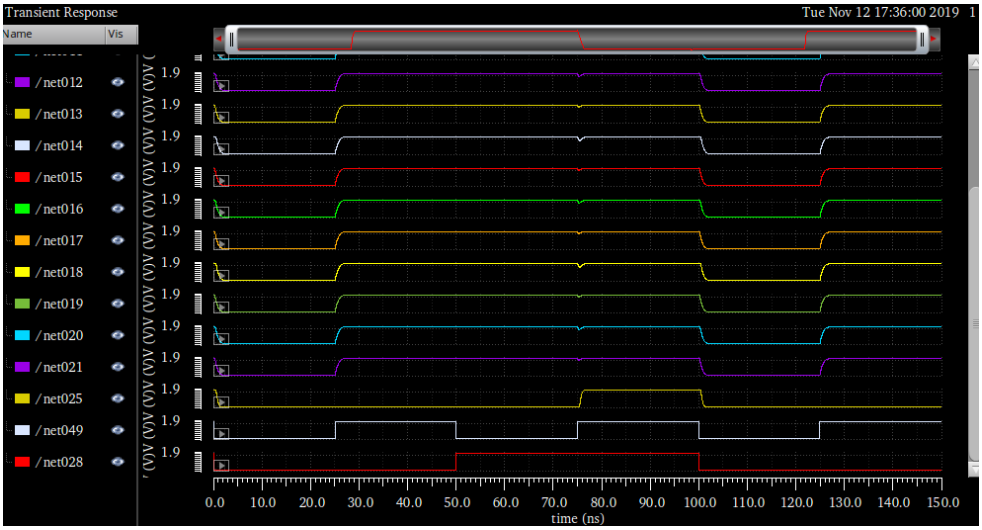

Figure 79: Simulation result of Schematic of first test - 2

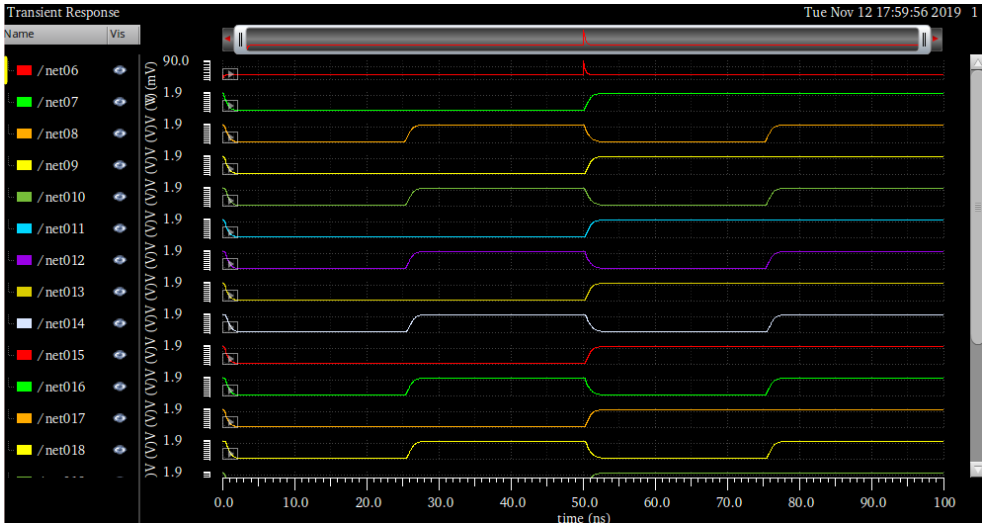

Figure 80: Simulation result of Schematic of second test - 1

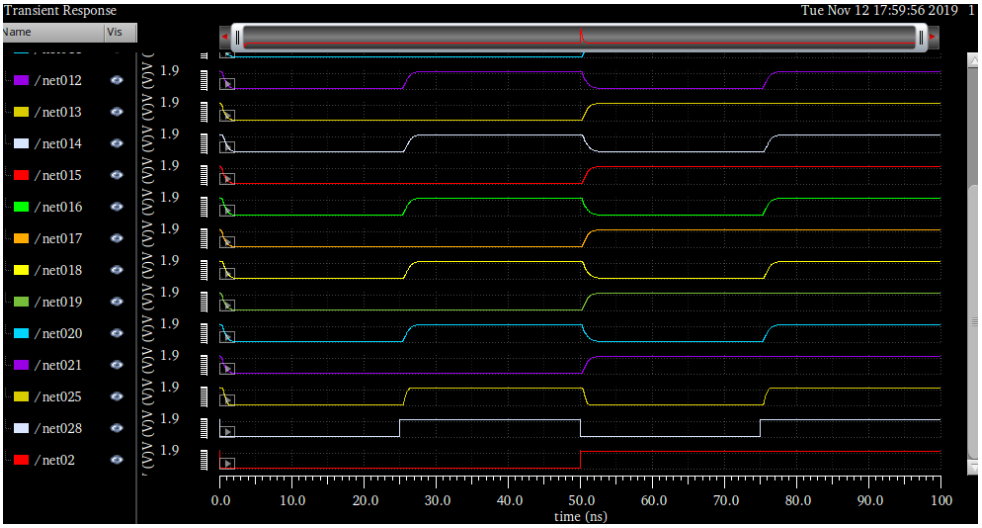

Figure 81: Simulation result of Schematic of second test - 2

3.

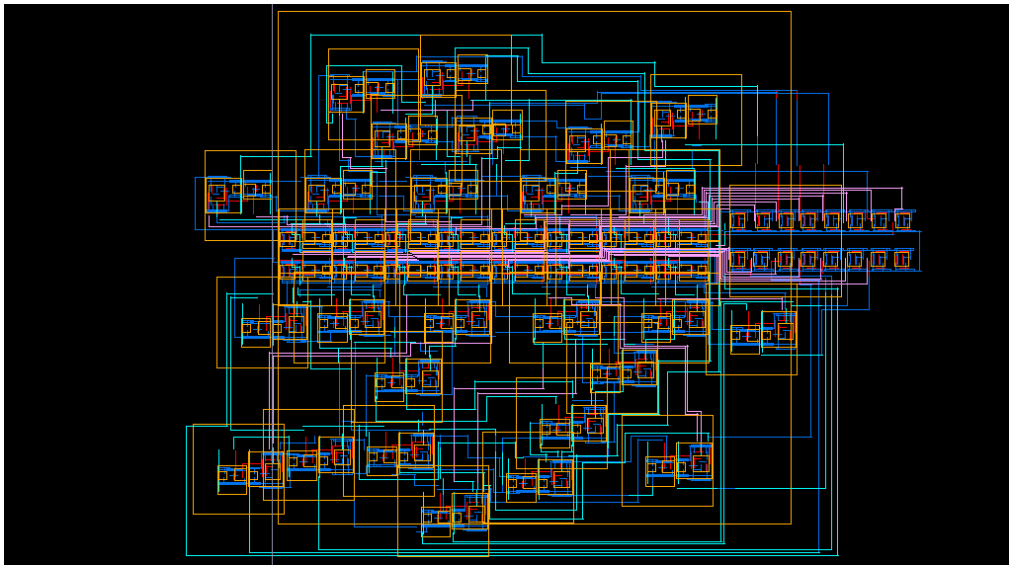

Figure 82: Layout of adder

4.

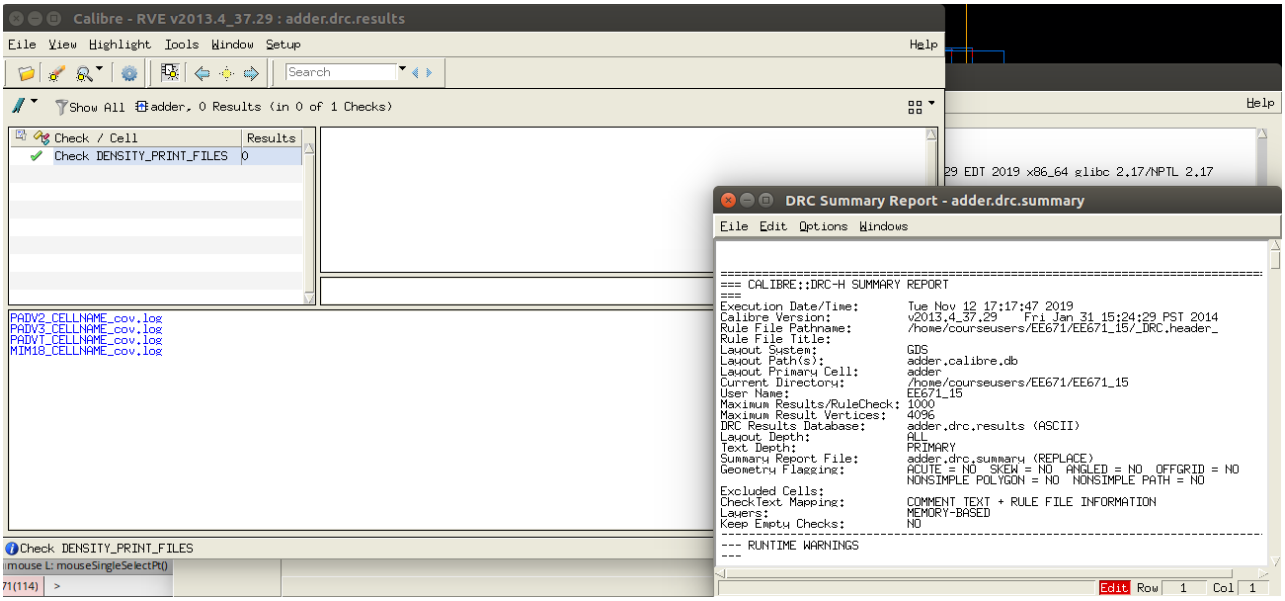

Figure 83: DRC of adder

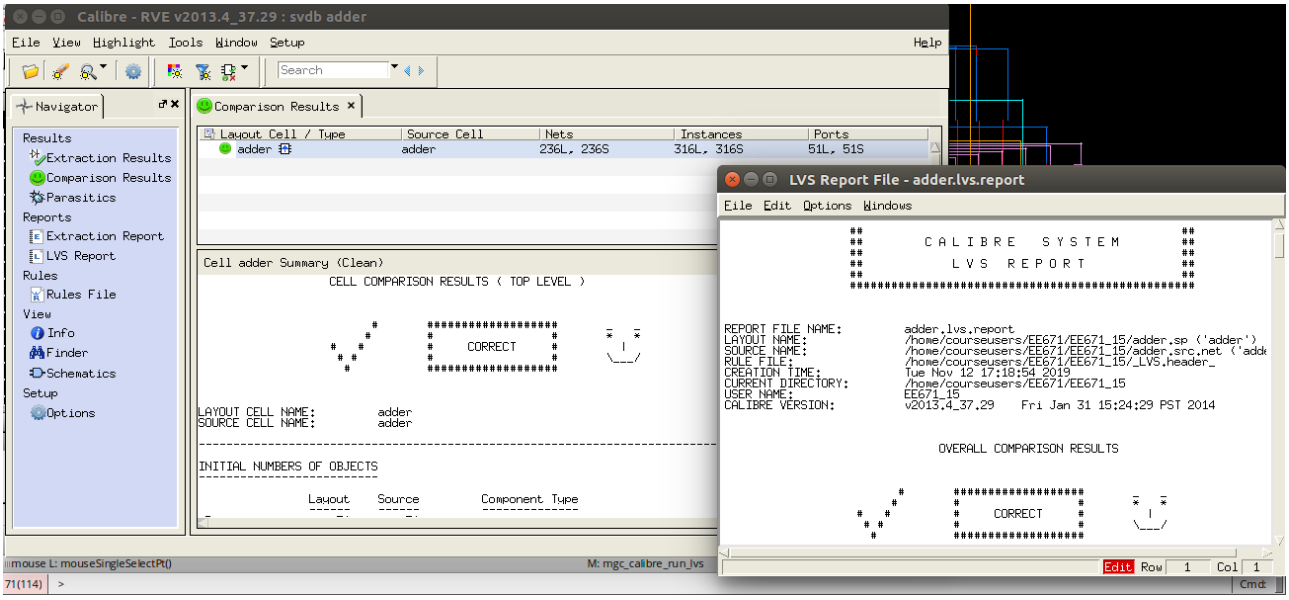

Figure 84: LVS of adder

5.

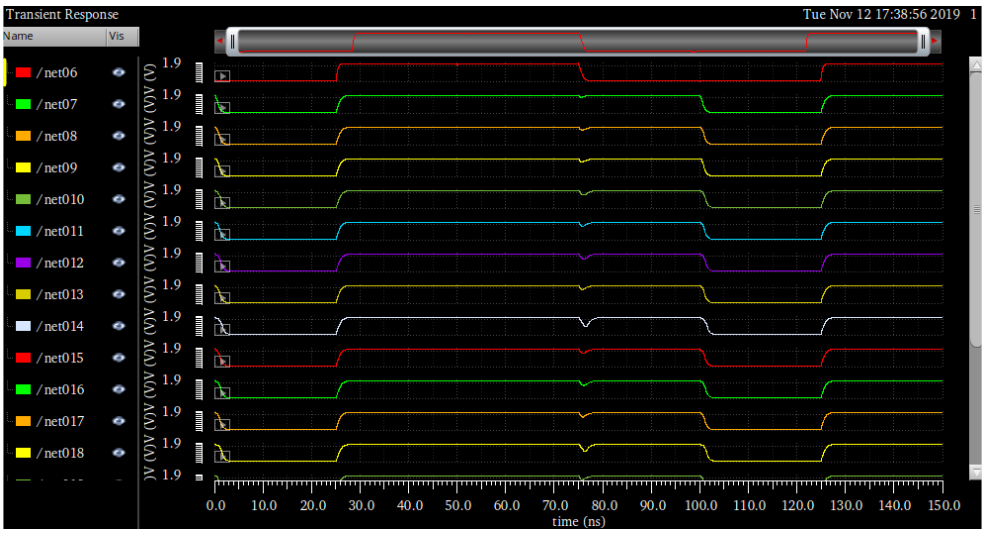

Figure 85: Simulation result of Layout for test 1 - 1

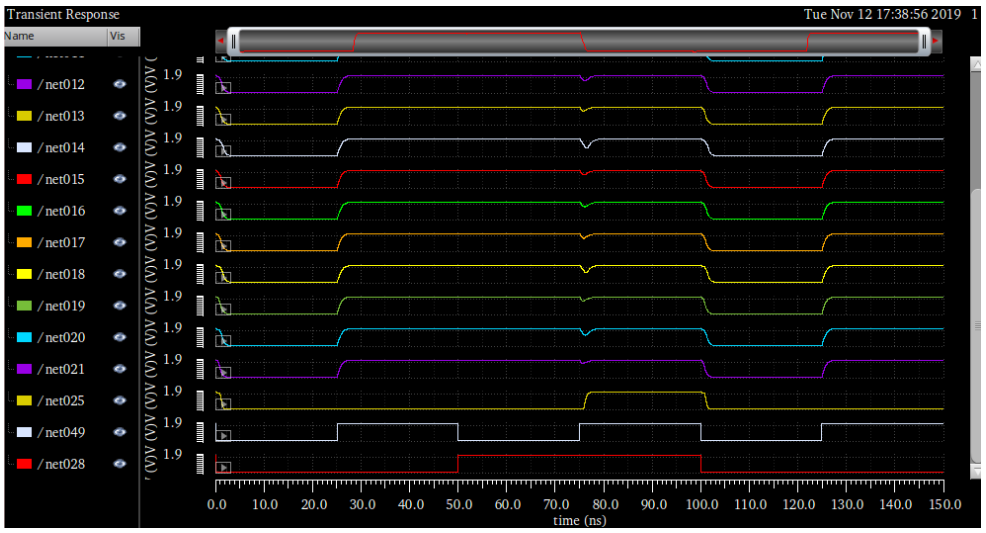

Figure 86: Simulation result of Layout for test 1 - 2

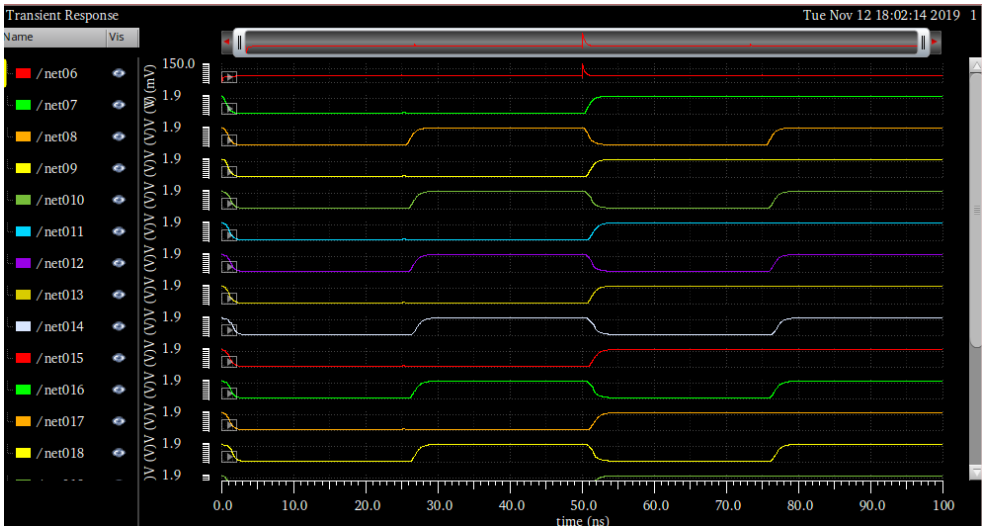

Figure 87: Simulation result of Layout for test 2 - 1

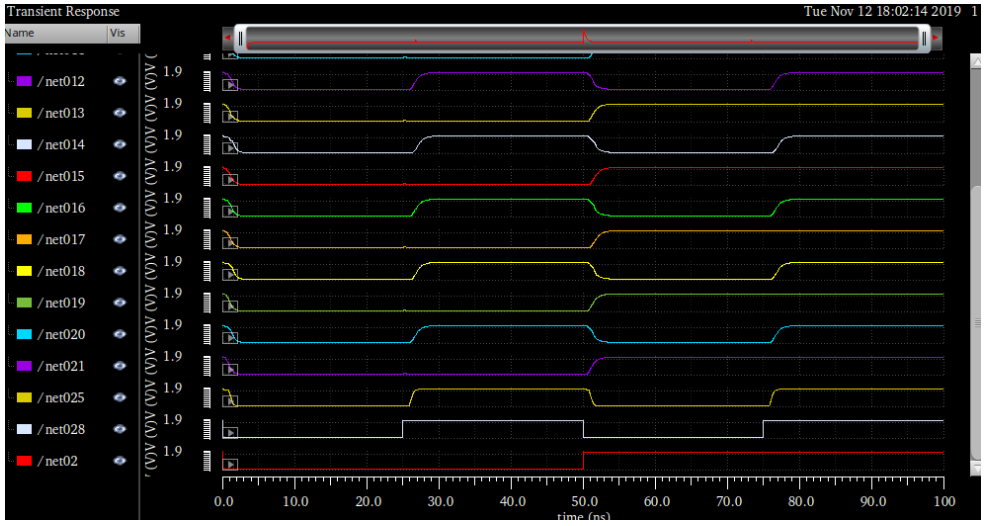

Figure 88: Simulation result of Layout for test 2 - 2

2 Worst Case Delay

For worst case delay, we keep one input as $2^{32} - 1$ and other as 1, and do calibre view (layout simulation). Here are all the outputs:

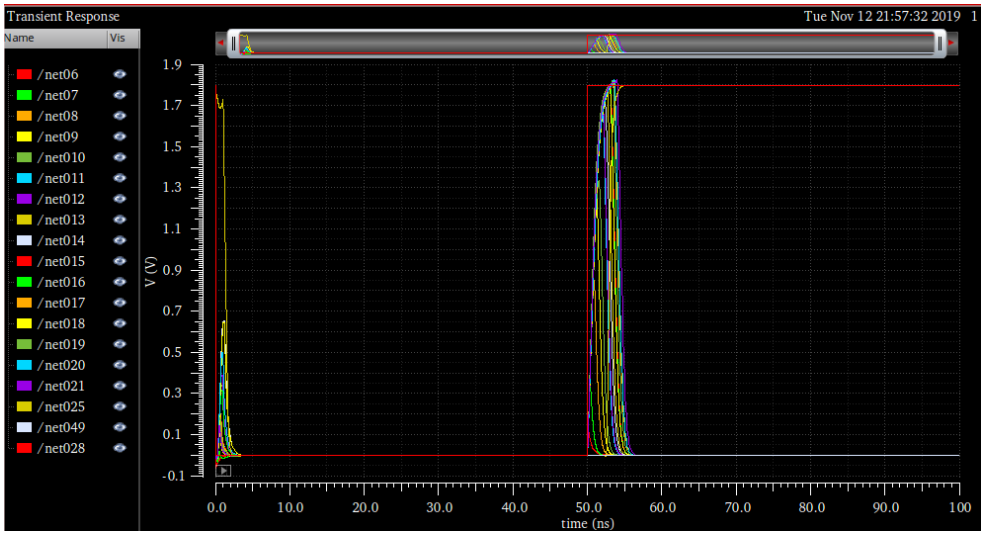

Figure 89: Simulation result of Layout for worst case delay

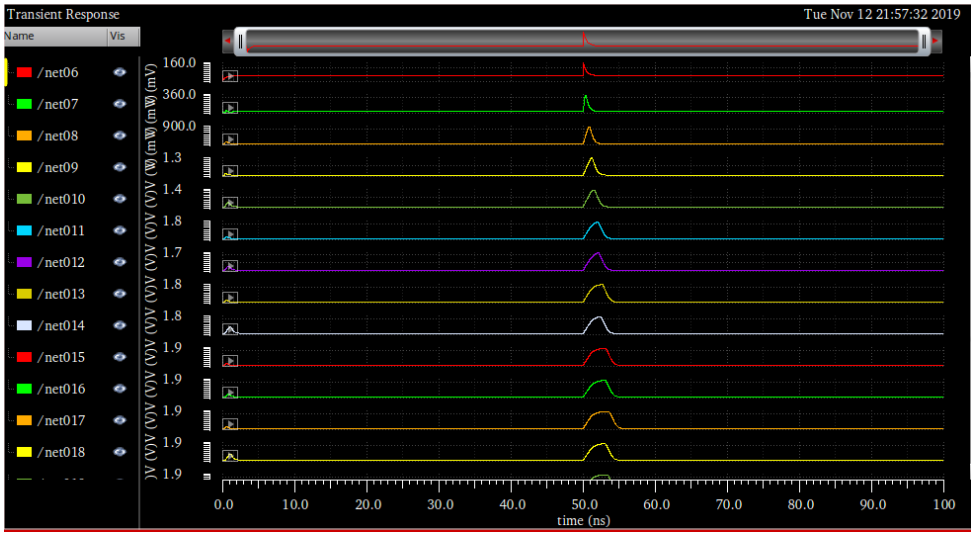

Figure 90: Simulation result of Layout for worst case delay

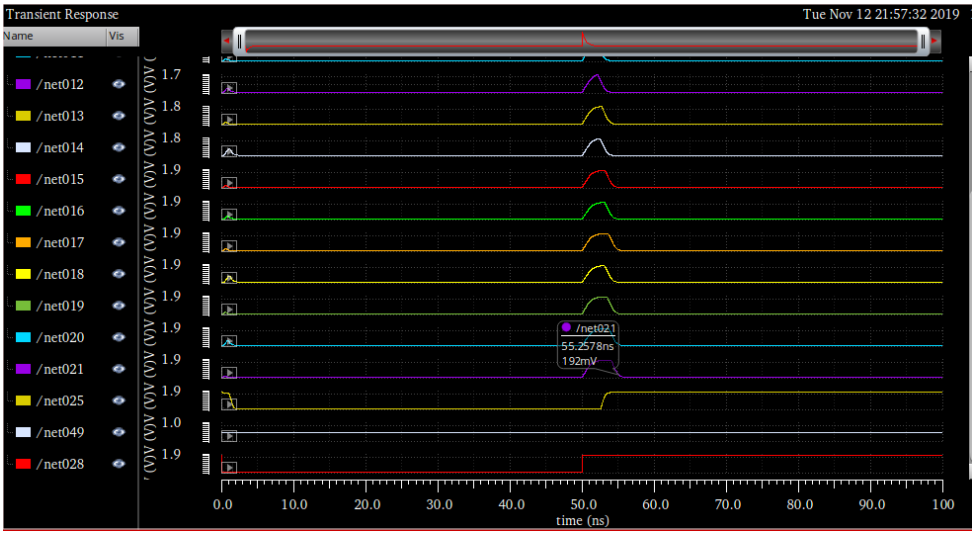

Figure 91: Simulation result of Layout for worst case delay

From the above figure we see that nearly 5.258 ns is required to reach nearly 0.18V for the worst case, i.e. for s_{15} to come (sum is $s_{16}s_{15}....s_0$) (note that net06 corresponds

to s_0 net07 to s_1 and so one till net021 corresponds to s_{15}; net025 corresponds to s_{16}; net049, net028 are inputs such that at 50 ns $2^{32} - 1$ and 1 are given as inputs)