## EE 671: Assignment 4 Report 16 bit Brent Kung Adder

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Directory: /home/courseusers/EE671/EE671\_15 In this directory, library assign4 has all the files.

#### 1 Order of figures for each module

1. Schematic of individual modules, whole 16 bit Brent Kung adder and their particular test benches.

2. Simulation results for the individual modules and whole adder.

3. The layout of individual modules and whole adder.

4. DRC and LVS report of individual modules and whole adder.

5. Post layout simulation results (In environment we append calibre, where calibre view was generated after pex of layout) for the individual modules and whole adder.

#### 1.1 Inverter/NOT gate: (NOT)



Figure 1: Schematic of NOT



Figure 2: Schematic of NOT\_test



Figure 3: Simulation result of Schematic



Figure 4: Layout of NOT

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Figure 6: LVS of NOT



Figure 7: Simulation result of Layout

#### 1.2 NAND gate: (NAND)



Figure 8: Schematic of NAND



Figure 9: Schematic of NAND\_test



Figure 10: Simulation result of Schematic

3.



Figure 11: Layout of NAND





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Figure 13: LVS of NAND



Figure 14: Simulation result of Layout

#### 1.3 AND gate: (AND)



Figure 15: Schematic of AND



Figure 16: Schematic of AND\_test



Figure 17: Simulation result of Schematic



Figure 18: Layout of AND

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Figure 20: LVS of AND



Figure 21: Simulation result of Layout

#### 1.4 $\overline{A + BC}$ gate: (some)



Figure 22: Schematic of some



Figure 23: Schematic of some\_test



Figure 24: Simulation result of Schematic





Figure 25: Layout of some

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Figure 26: DRC of some

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Figure 27: LVS of some



Figure 28: Simulation result of Layout

## 1.5 A + BC gate: (somen)



Figure 29: Schematic of somen



Figure 30: Schematic of somen\_test





Figure 31: Simulation result of Schematic



Figure 32: Layout of somen

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Figure 34: LVS of somen



Figure 35: Simulation result of Layout

#### 1.6 Tiny XOR gate: (xor)



Figure 36: Schematic of xor



Figure 37: Schematic of xor\_test



Figure 38: Simulation result of Schematic





Figure 39: Layout of xor

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Figure 40: DRC of xor

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Figure 41: LVS of xor



Figure 42: Simulation result of Layout

#### **1.7** Calculating $P_i$ and $G_i$ from inputs: (pg1)



Figure 43: Schematic of pg1



Figure 44: Schematic of pg1\_test



Figure 45: Simulation result of Schematic



Figure 46: Layout of pg1



Figure 47: DRC of pg1

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Figure 48: LVS of pg1



Figure 49: Simulation result of Layout

## 1.8 Block of 16 pg1: (propgrop1)



Figure 50: Schematic of propgrop1



Figure 51: Schematic of propgrop1\_test - Propagation



Figure 52: Schematic of propgrop1\_test - Generation

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Figure 53: Simulation result of Schematic-Propagation

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Figure 54: Simulation result of Schematic-Generation



Figure 55: Layout of propgrop1

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Figure 57: LVS of propgrop1

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Figure 58: Simulation result of Layout - Propagation



Figure 59: Simulation result of Layout - Generation

# **1.9** Next P and G Calculator from $P_i, G_i, P_{i-1}, G_{i-1}$ : (pg)



Figure 60: Schematic of pg



Figure 61: Schematic of  $pg\_test$ 



Figure 62: Simulation result of Schematic



Figure 63: Layout of pg

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Figure 65: LVS of pg



Figure 66: Simulation result of Layout

#### 1.10 16 xor gate set for final sum calculation: (prop)



Figure 67: Schematic of prop



Figure 68: Schematic of prop\_test



Figure 69: Simulation result of Schematic





Figure 70: Layout of prop

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Figure 71: DRC of prop

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Figure 72: LVS of prop



Figure 73: Simulation result of Layout

#### 1.11 Adder: (adder)



Figure 74: Schematic of adder



Figure 75: Schematic of proc block of Adder

We have two test adders. First is for the 0-0, 0-65535, 65535-0, 65535-65535 cases and next has alternate bits being 1 and 0.



Figure 76: Schematic of first adder\_test (adder\_test)



Figure 77: Schematic of second adder\_test (adder\_test1)



Figure 78: Simulation result of Schematic of first test - 1

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/net028	0	5 1.9		
			0.0 10.0 20.0 30.0 40.0 50.0 60.0 70.0 80.0 90.0 100.0 110.0 time (rs)	120.0 130.0 140.0 150.0

Figure 79: Simulation result of Schematic of first test - 2



Figure 80: Simulation result of Schematic of second test - 1



Figure 81: Simulation result of Schematic of second test - 2



Figure 82: Layout of adder



Figure 83: DRC of adder

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Figure 84: LVS of adder



Figure 85: Simulation result of Layout for test 1 - 1



Figure 86: Simulation result of Layout for test 1 - 2

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Figure 87: Simulation result of Layout for test 2 - 1



Figure 88: Simulation result of Layout for test 2 - 2

#### 2 Worst Case Delay

For worst case delay, we keep one input as  $2^{32} - 1$  and other as 1, and do calibre view (layout simulation). Here are all the outputs:



Figure 89: Simulation result of Layout for worst case delay



Figure 90: Simulation result of Layout for worst case delay



Figure 91: Simulation result of Layout for worst case delay

From the above figure we see that nearly 5.258 ns is required to reach nearly 0.18V for the worst case, i.e. for  $s_{15}$  to come (sum is  $s_{16}s_{15}...s_0$ ) (note that net06 corresponds

to  $s_0$  net07 to  $s_1$  and so one till net021 corresponds to  $s_{15}$ ; net025 corresponds to  $s_{16}$ ; net049, net028 are inputs such that at 50 ns  $2^{32} - 1$  and 1 are given as inputs)