Report

1. Circuit and description of operation including hand analyses.
- circuit: page 12
- hand analyses: page 15 onwards
- table of parameters hand analysis vs SPICE: page 14

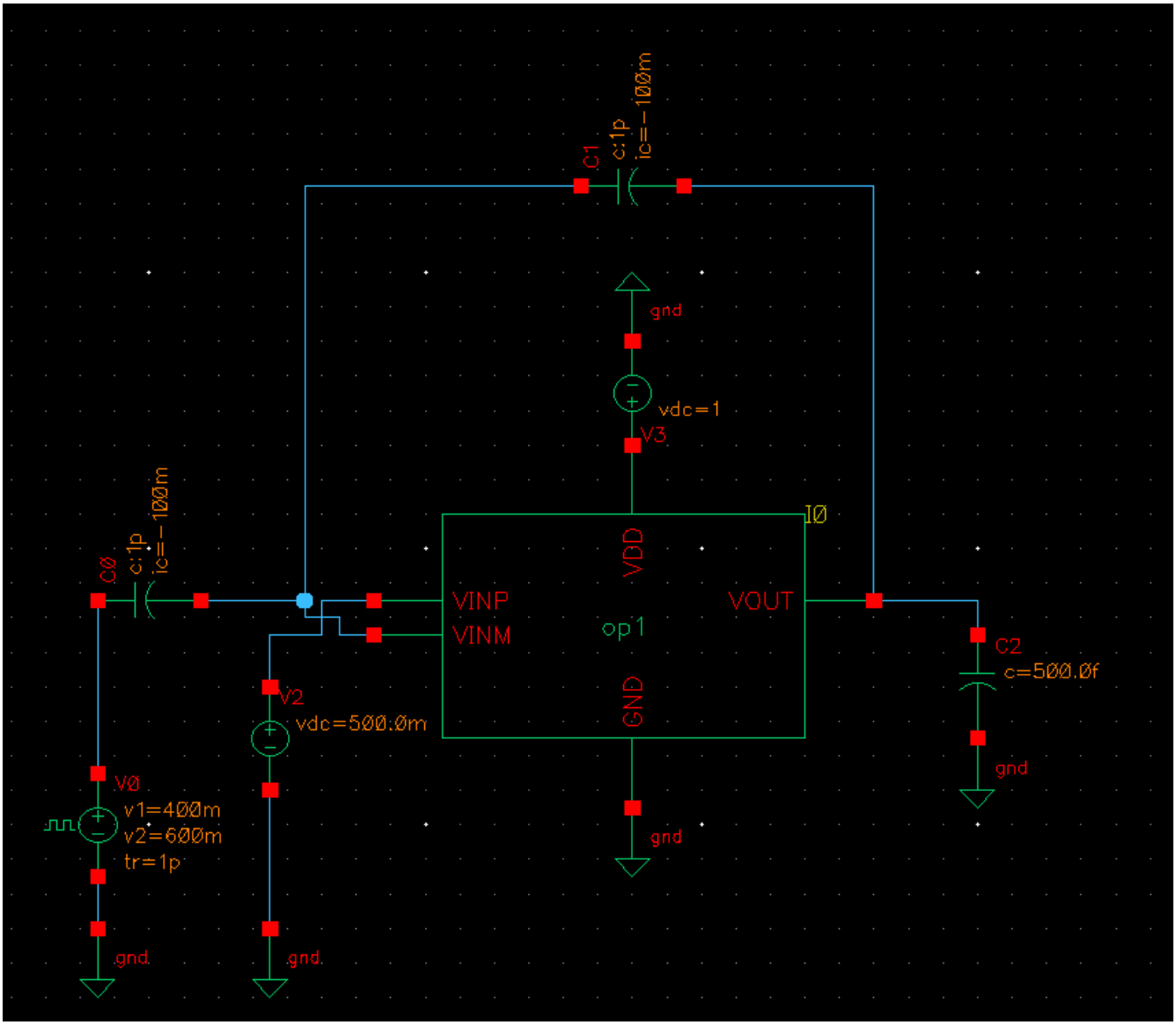
2. SPICE or Cadence outputs. Fit each output graph on one page. Submit zoomed-in figures for settling time simulations to demonstrate 0.5% settling in both directions.
- all specifications from pages 2-11

3. Table comparing SPICE performance with design objectives.
- page 13

4. Discussion of circuit performance with special attention to unique areas in your design which helped/hurt your specs.
- page 13

Specification 1: Met
Maximum Settling Time: 8.0ns/8.0ns to within 0.5% of the output step size, settling up/settling down (output going up AND down). You need to meet specs in both directions.

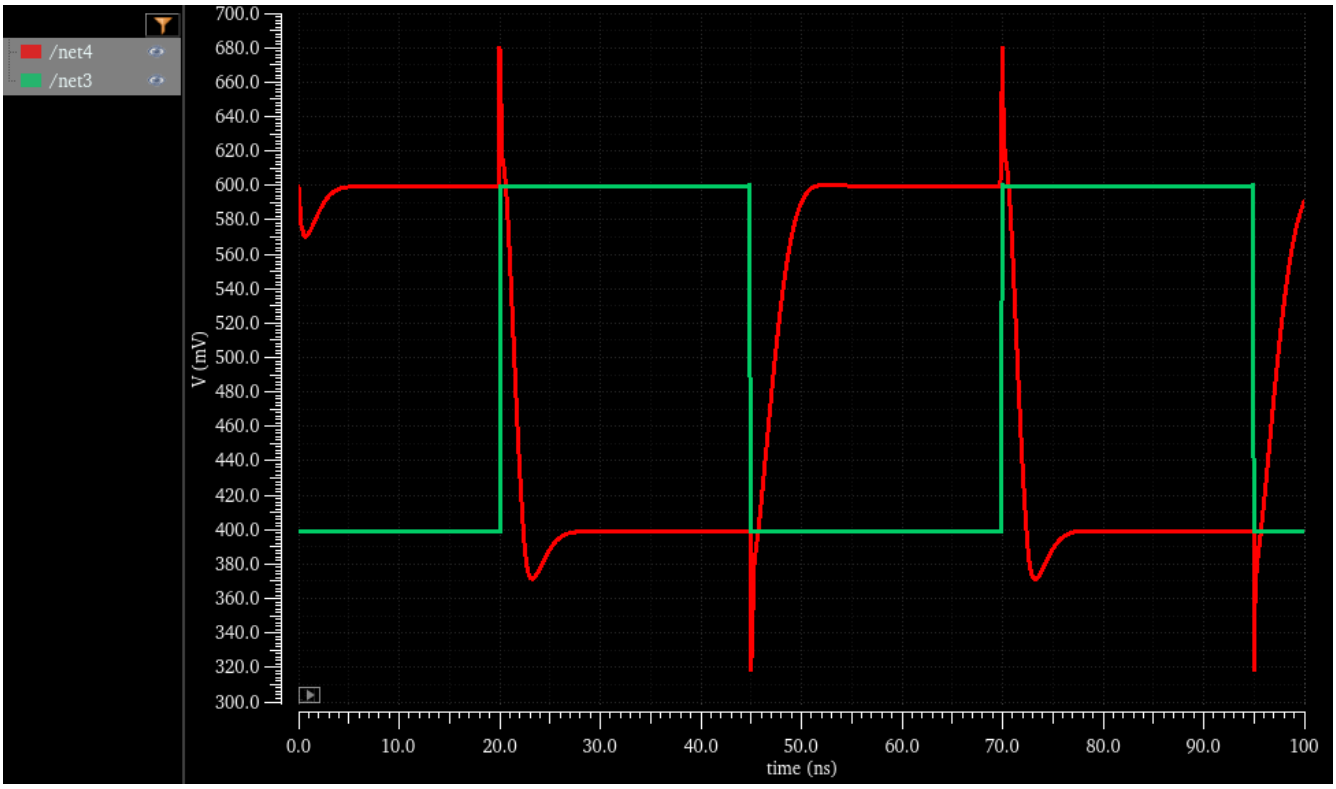
Testbench:



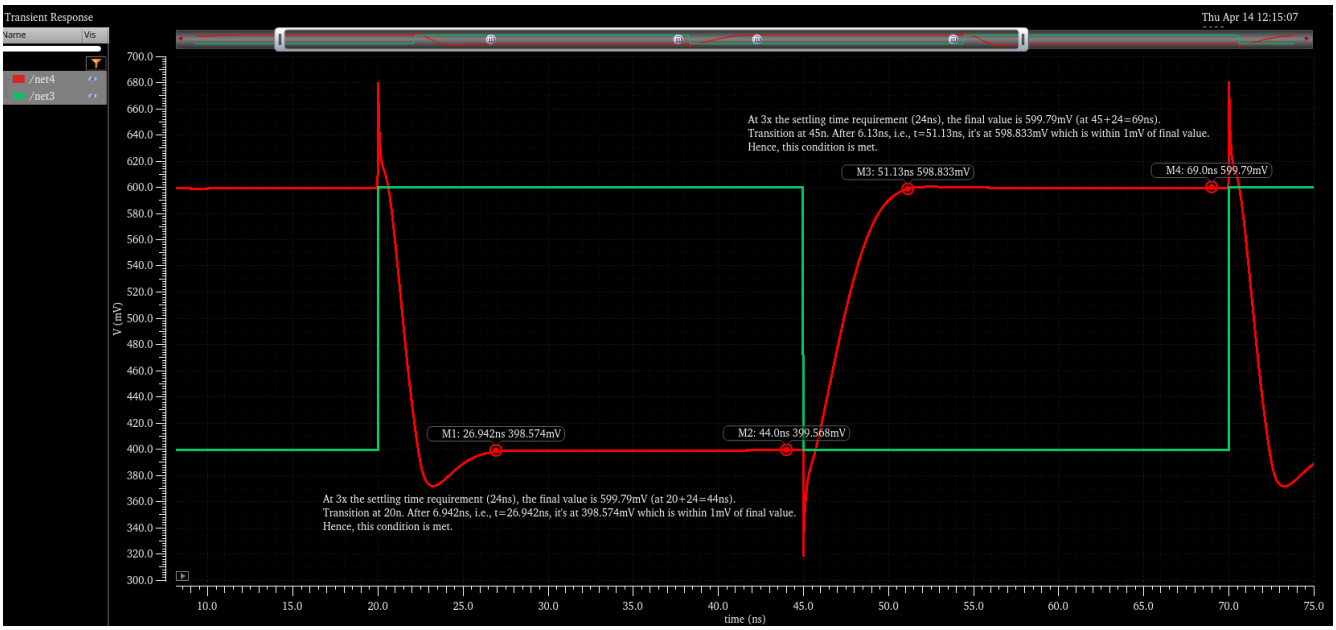
Result:

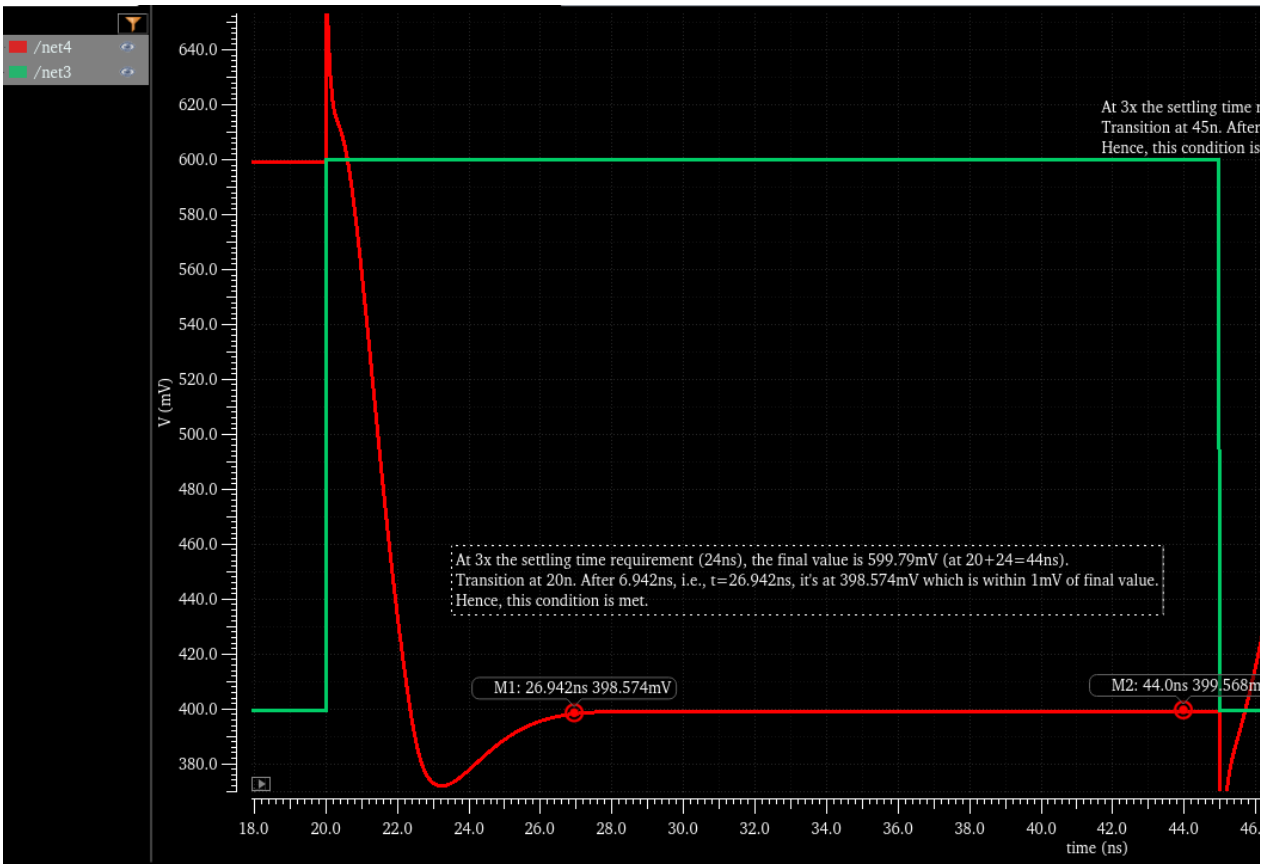
	Name/Signal/Expr	Value	Plot	Save	Sa
1	vout_net4		☑	☐	allv
2	t_settle1	6.942n	☑	☐	
3	vin_net3		☑	☐	allv
4	t_settle2	6.113n	☑	☐	

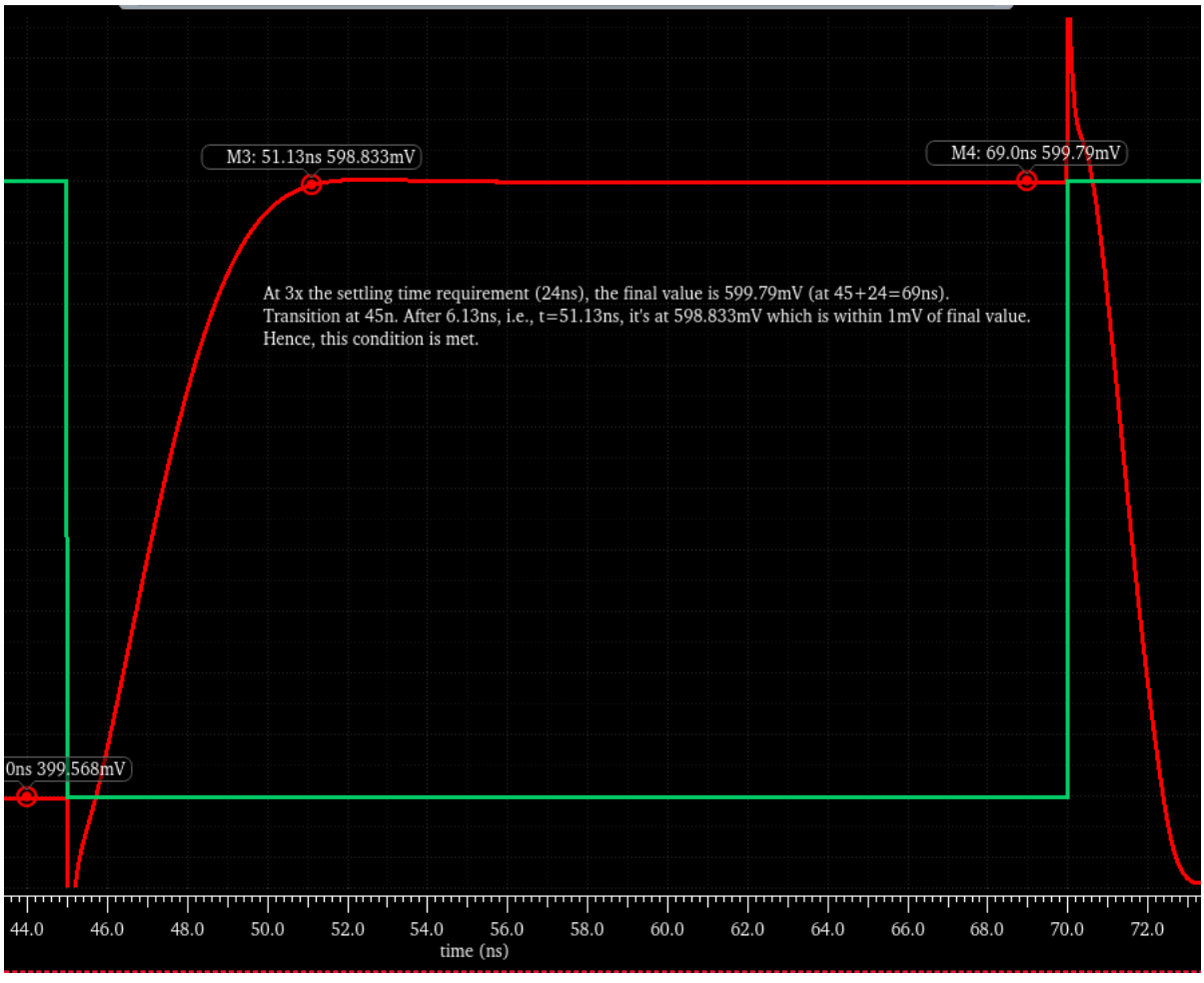
where
t_settle1 = (settlingTime(v("/net4" ?result "tran") 2e-08 t 4.5e-08 t 0.5) – 2.0005e-08)
t_settle2 = (settlingTime(v("/net4" ?result "tran") 4.5e-08 t 7e-08 t 0.5) - 4.5005e-08)



Zoomed in results:

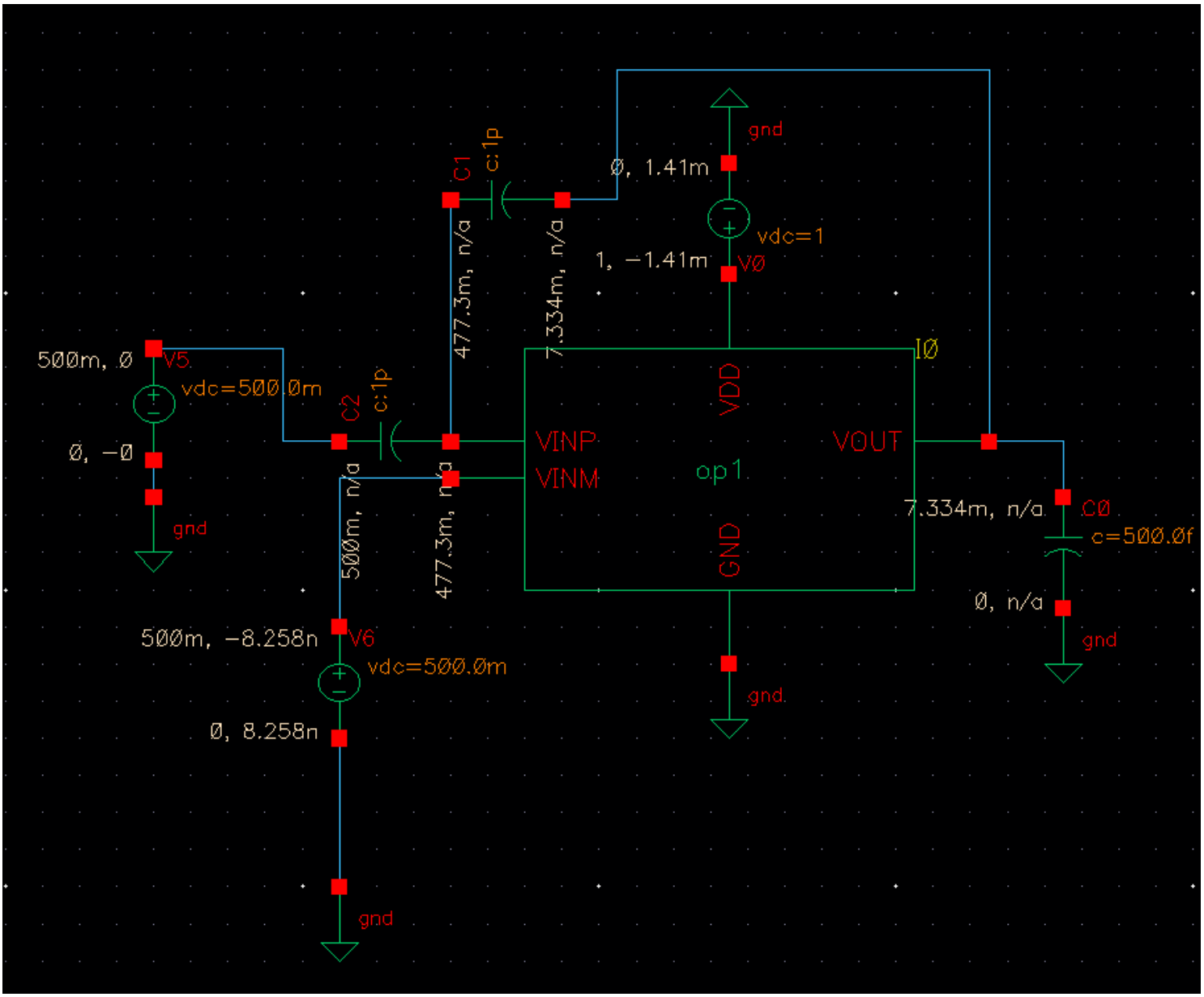



/net4
/net3
640.0
620.0
600.0
580.0
560.0
540.0
520.0
500.0
480.0
460.0
440.0
420.0
400.0
380.0
V (mV)
At 3x the settling time
Transition at 45n. After
Hence, this condition is
At 3x the settling time requirement (24ns), the final value is 599.79mV (at 20+24=44ns).
Transition at 20n. After 6.942ns, i.e., t=26.942ns, it's at 398.574mV which is within 1mV of final value.
Hence, this condition is met.
M1: 26.942ns 398.574mV
M2: 44.0ns 399.568m
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0
34.0
36.0
38.0
40.0
42.0
44.0
time (ns)


M3: 51.13ns 598.833mV
M4: 69.0ns 599.79mV
At 3x the settling time requirement (24ns), the final value is 599.79mV (at 45+24=69ns).
Transition at 45n. After 6.13ns, i.e., t=51.13ns, it's at 598.833mV which is within 1mV of final value.
Hence, this condition is met.
0ns 399.568mV
44.0
46.0
48.0
50.0
52.0
54.0
56.0
58.0
60.0
62.0
64.0
66.0
68.0
70.0
72.0
time (ns)

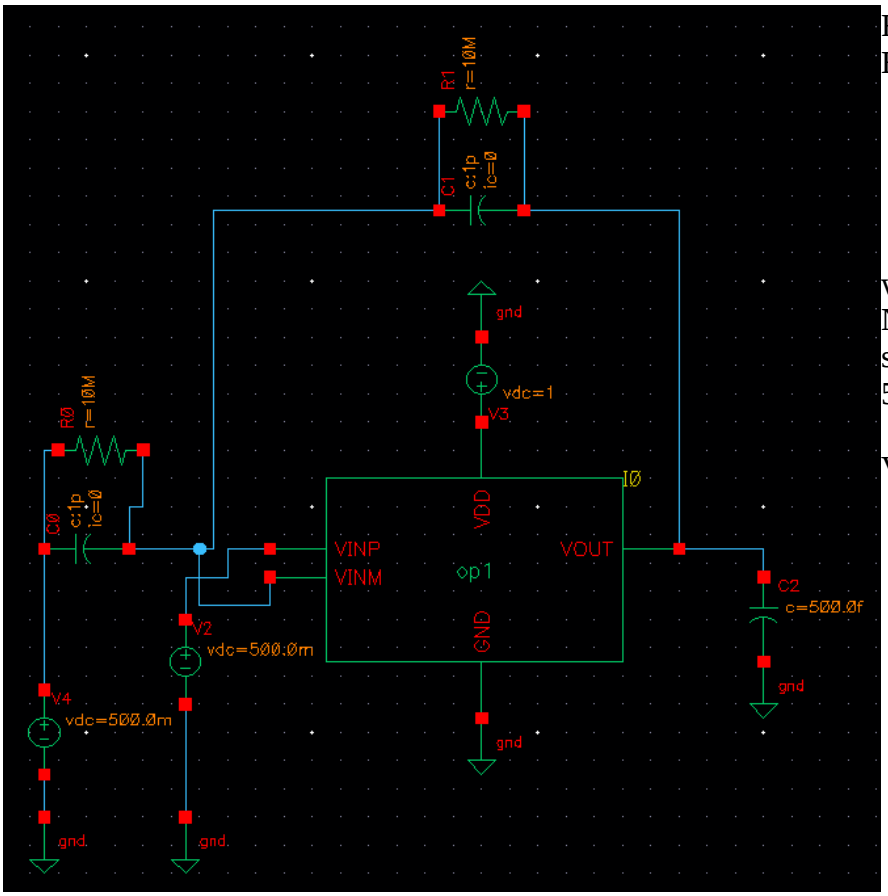
Specification 2: Met
DC Power Consumption measured with VIN=0.5 and (VOUT=0.5) in Fig. 1: 1.5mW. Includes power from the 1.0 and 0.5 volt supplies, and the ideal current source.

Testbench and result:



No current source used in design. Only this one DC source of 1V and CM of 0.5V.
DC source power: 1.41mA*1V = 1.41mW
0.5V CM power: 8.258nA*0.5V = 4.129nW
Total power ~ 1.41 mW < 1.5 mW

Specification 3: Met
Thermal Noise: < 300 uV rms, output referred, in the configuration shown in Fig. 1.
Integrate output noise from 1MHz to 500 MHz.
Testbench:

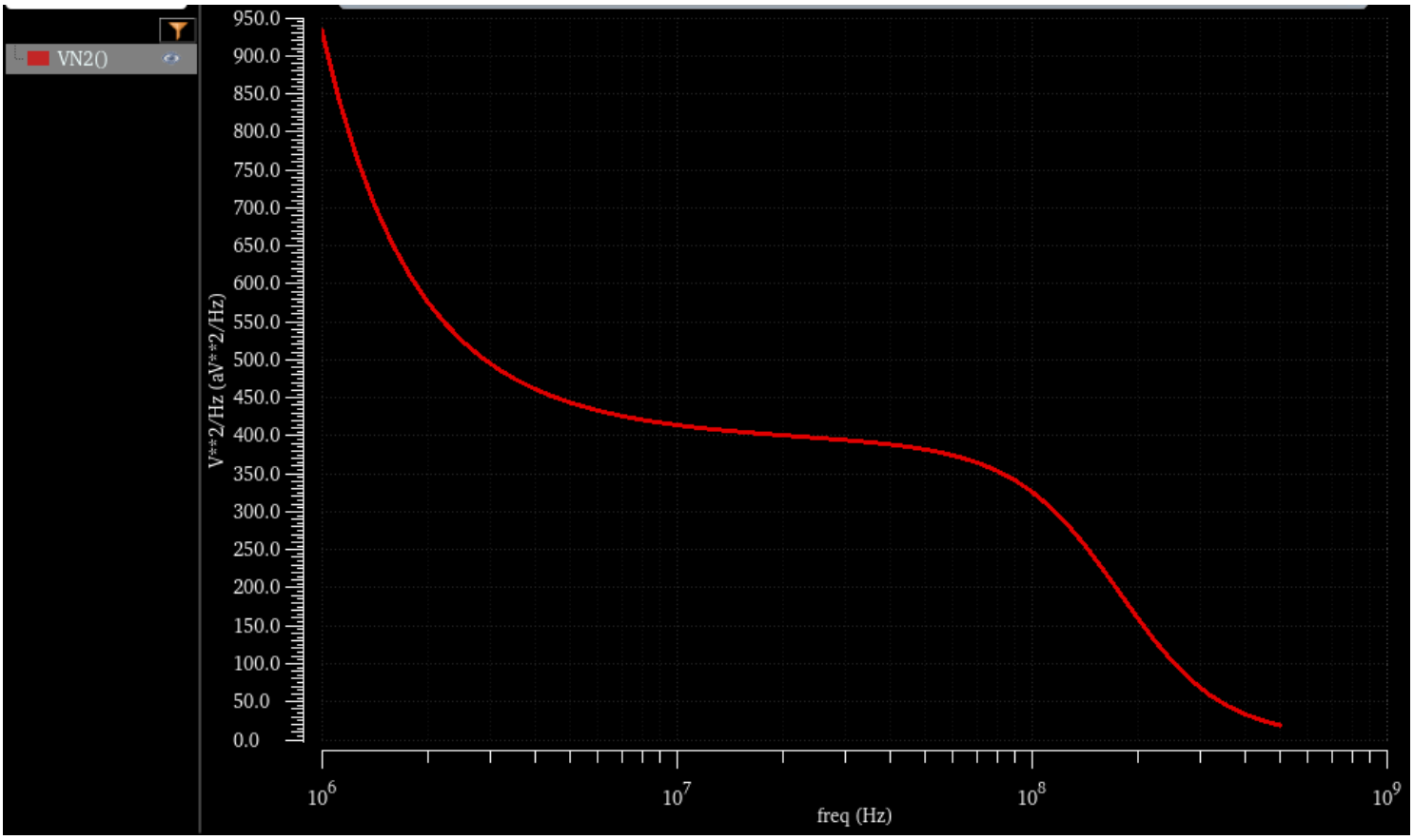


Results:
By two methods, noise = 284.5u<300u

	Name/Signal/Expr	Value	Plot	Save
1	Noise_rms	284.5u	☑	☐
2	sqrt_integrate_PSD	284.5u	☑	☐

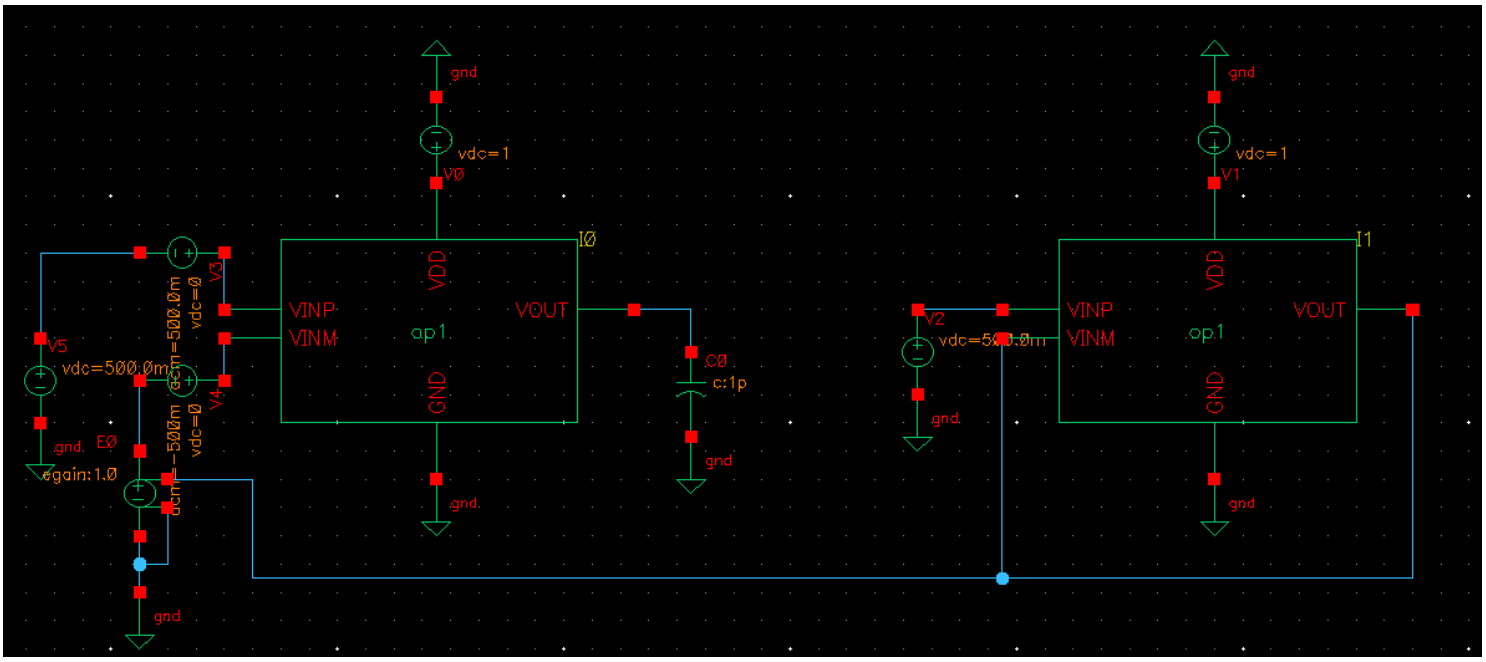
where
Noise_rms = rmsNoise(1000000 500000000)
sqrt_integrate_PSD = sqrt(integ(VN2() 1000000 500000000 " "))

VN2 is plotted below:

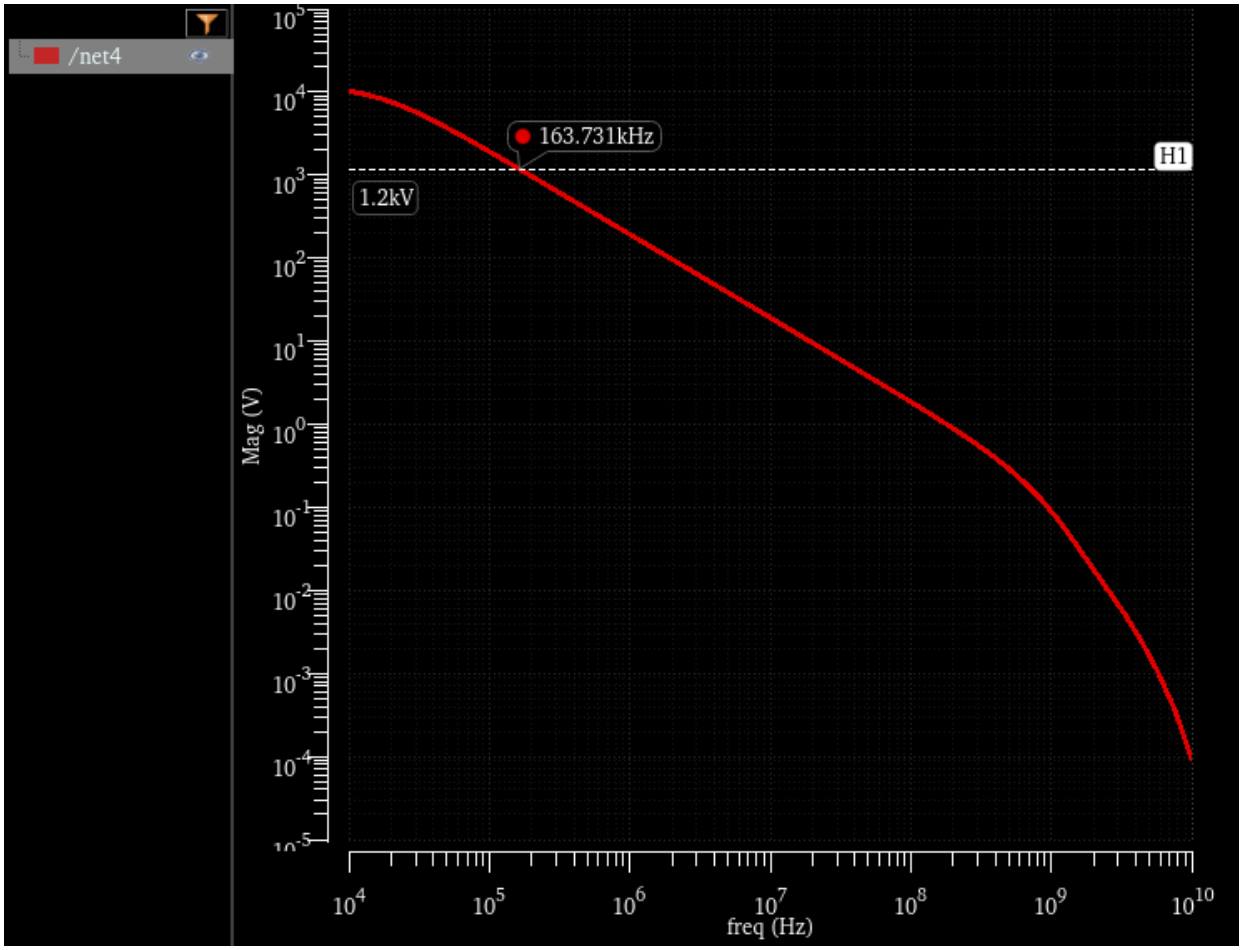


Specification 4: Met
DC Small Signal Differential Gain (measured open-loop): > 1,200

Testbench:



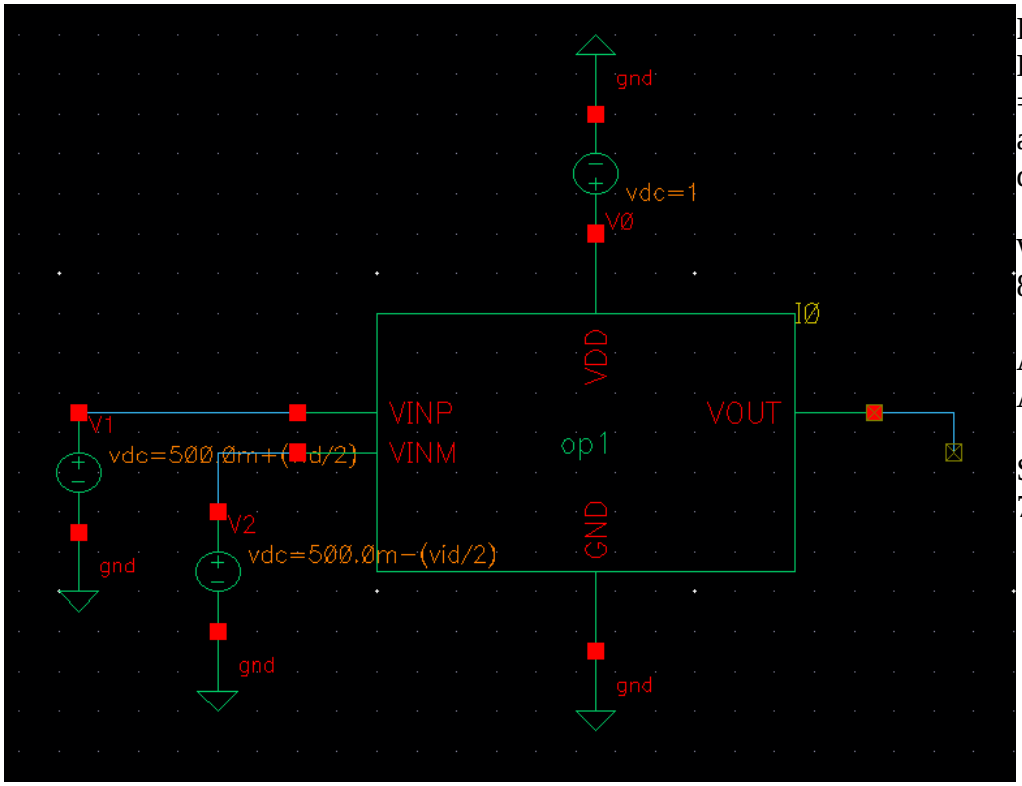
Results:



At 10kHz, gain of 10336.5. Gain>1200 till 163.731kHz.

Specification 5: Met
Output Swing (measured open-loop without any load): Within 0.25 V of both VDD=1.0 and AGND=0. (Defined as max. output range for which the incremental gain vo/vid is still at least 500)

Testbench:

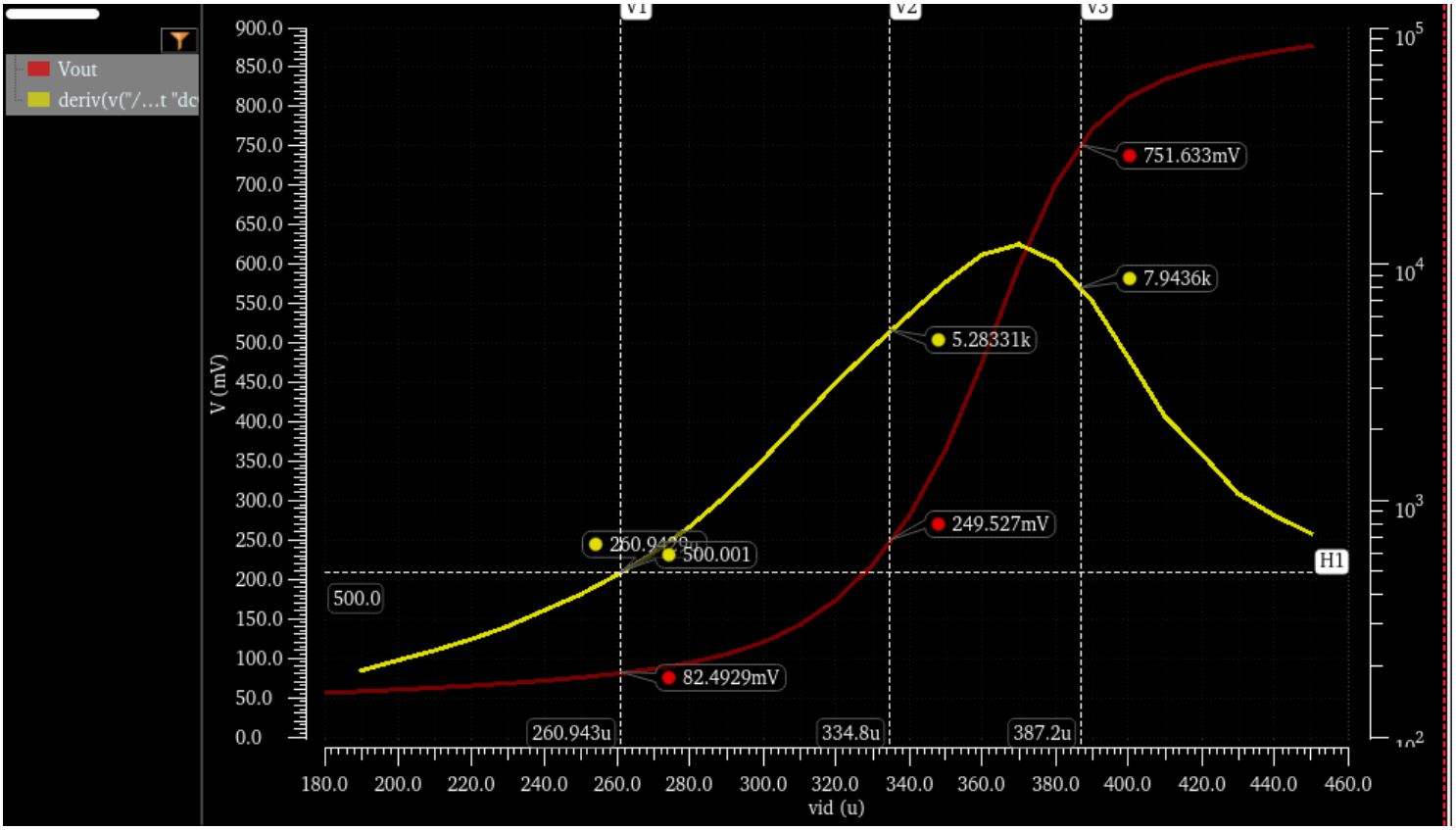


Results:
Due to offset, we simulate from vid = 180u to 450u
and plot derivative of Vout or /net2: deriv(v("/net2" ?result "dcOp")).

We see an output swing of 82.4929mV to 1V where gain>500.

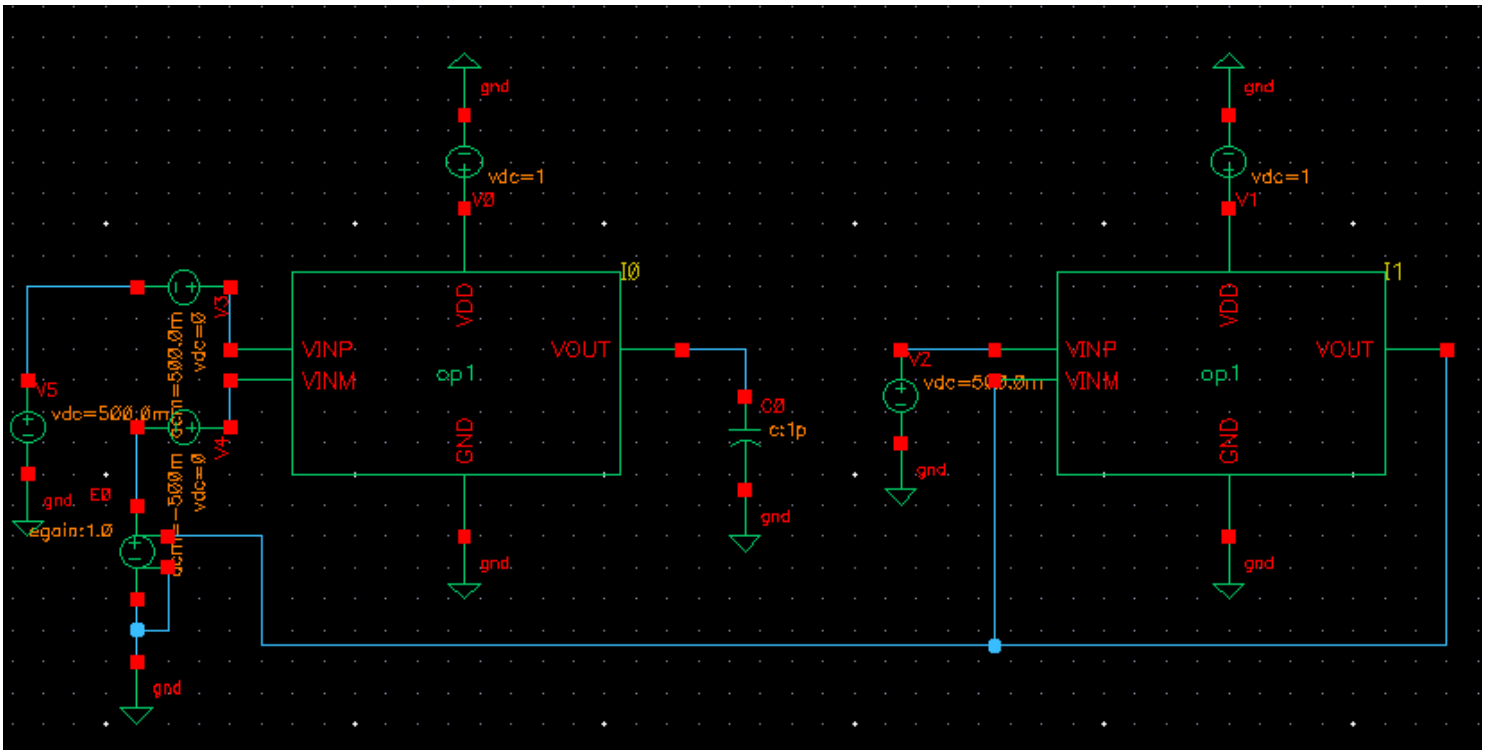
At 249.527mV, gain=5.28331k
At 751.633mV, gain=7.9436k

So, for Vout between 250mV and 750mV, gain>500.

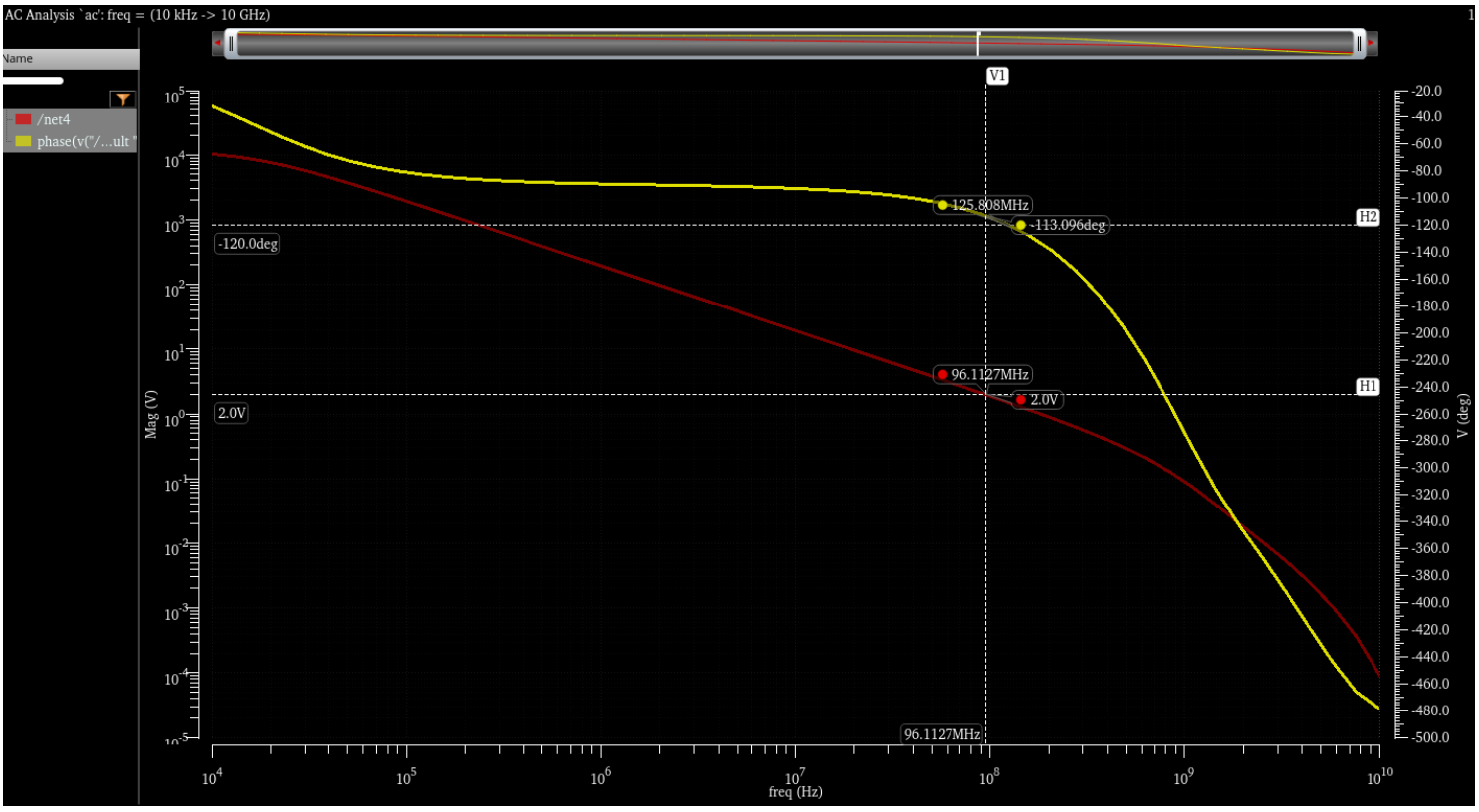


Specification 6: Met
Phase Margin 1pF load: At least 60deg at the feedback factor f=0.5 (i.e., gain-of-2 crossover).

Testbench:



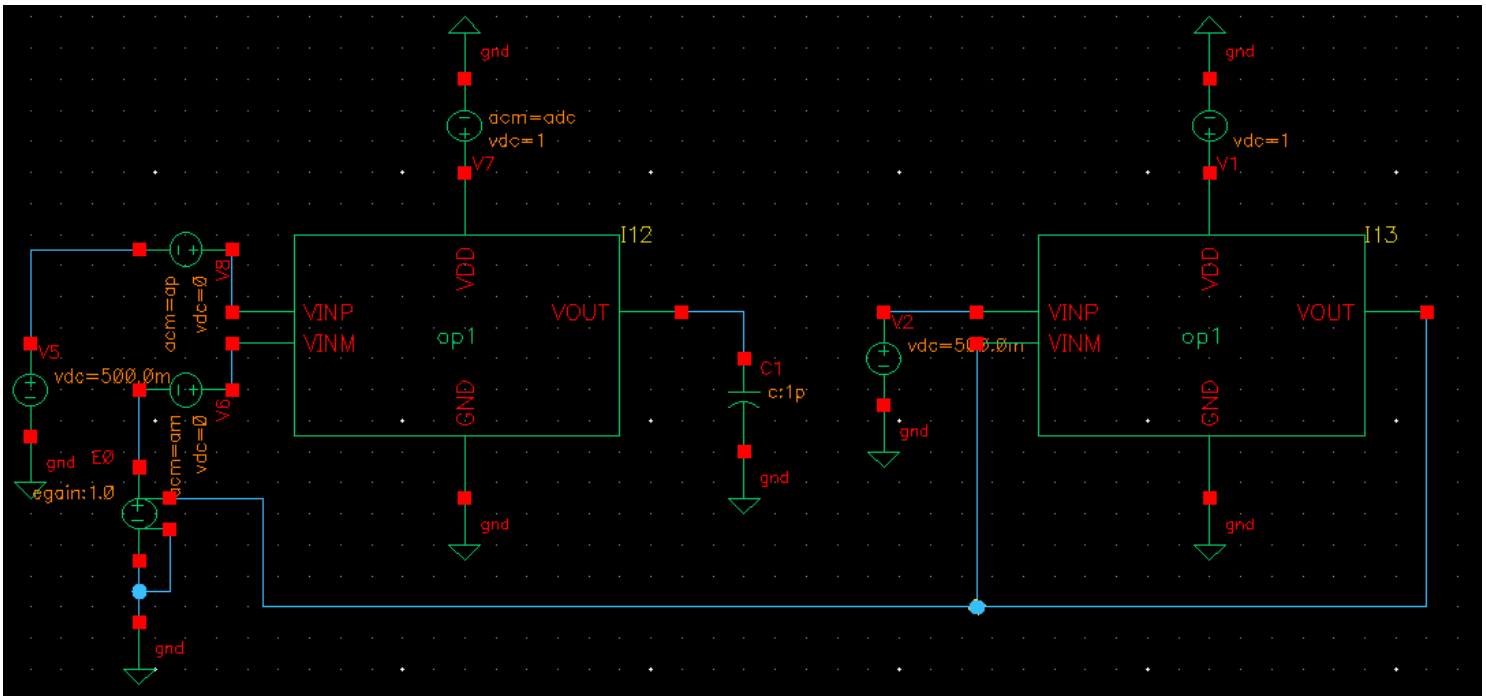
Results:



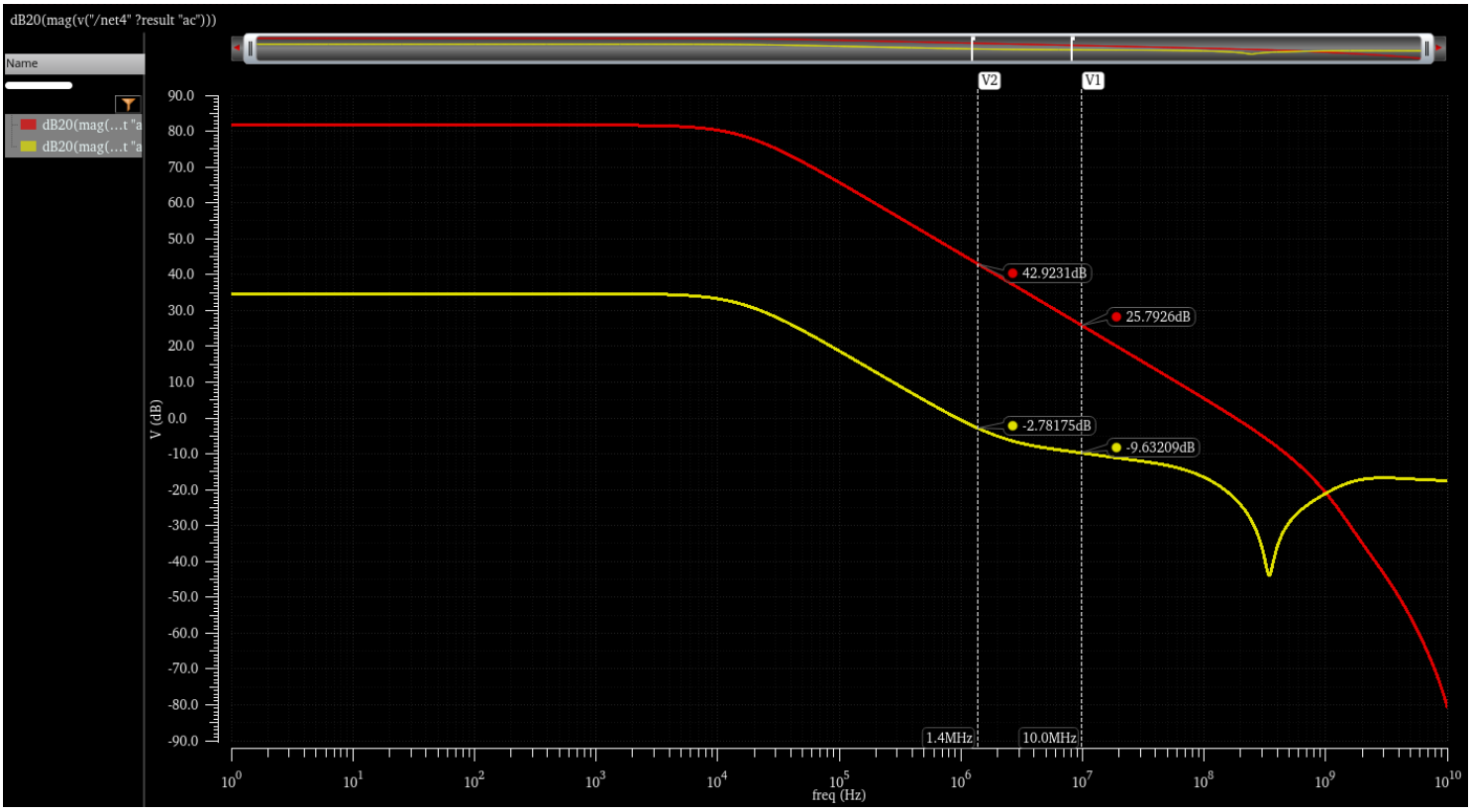
Phase margin of 66.904 deg at gain-of-2 crossover frequency of 96.1127MHz. Phase margin of 60 deg at 125.808MHz where the gain is 1.51134.

Specification 7: Not Met (35dB instead of 40dB)
PSRR+(from VDD) >40 dB at DC-10MHz

Testbench:



Results:

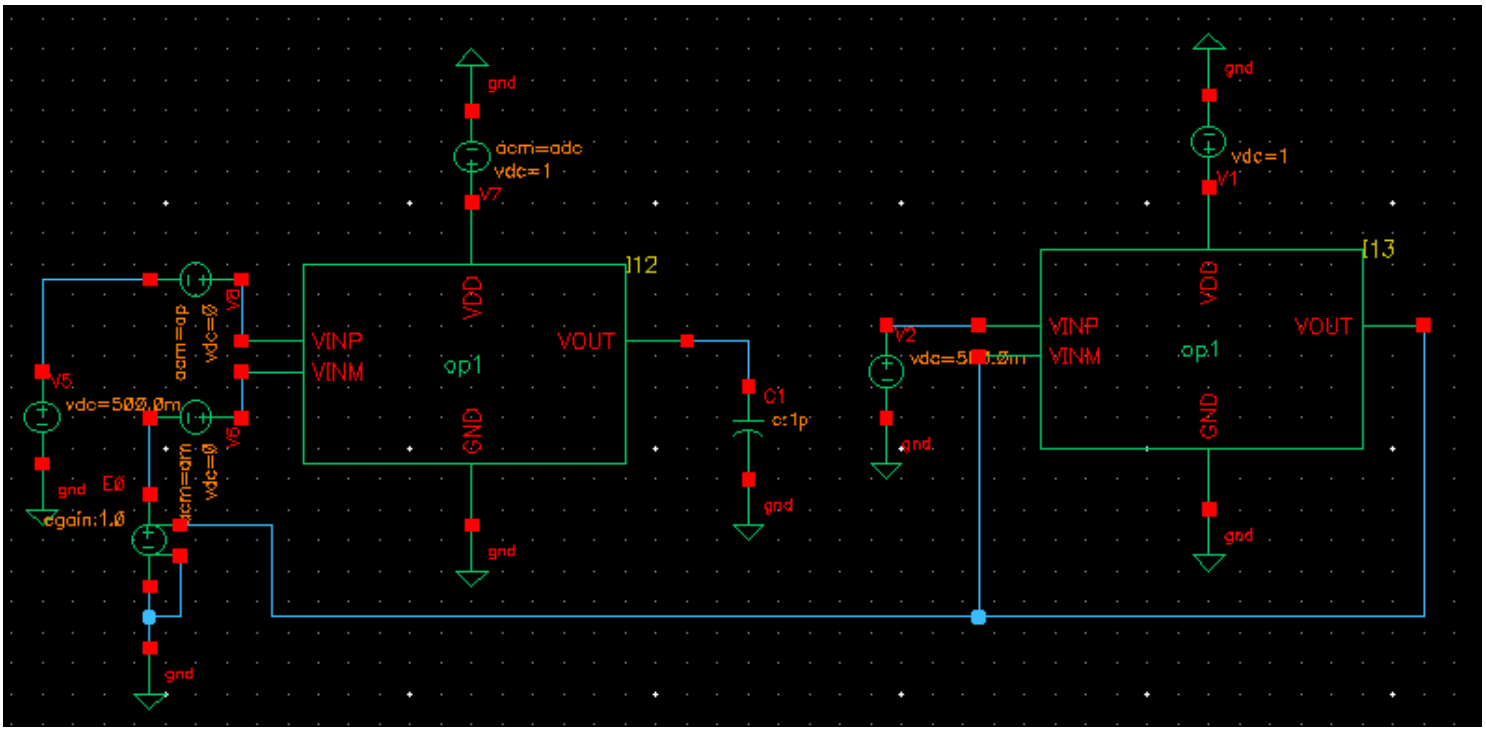


Red curve: ap = 0.5V, am = -0.5V, adc = 0V
Yellow curve: ap = 0V, am = 0V, adc = 1V

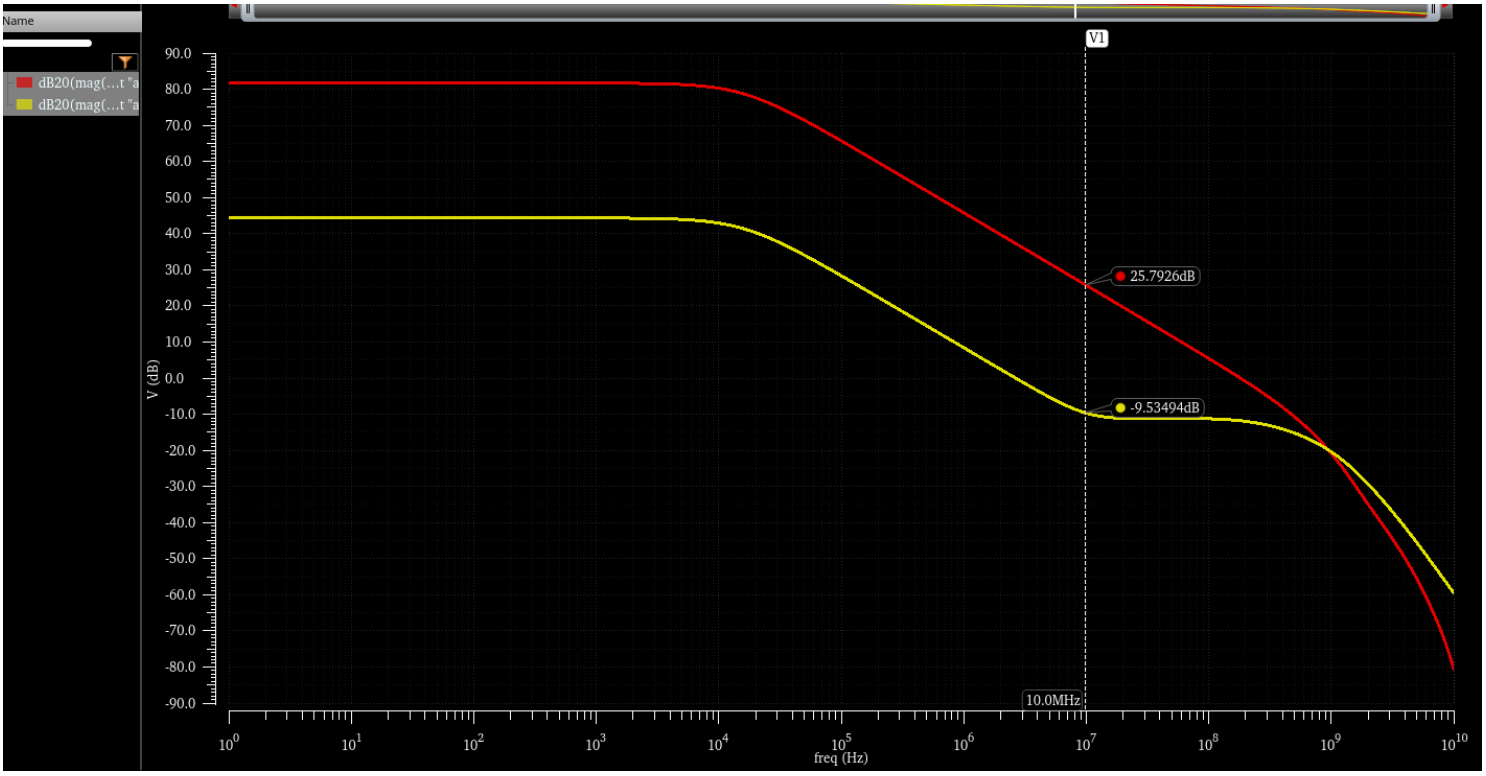
40dB till 1.4MHz
35.42469dB at 10MHz

Specification 8: Not Met (35dB instead of 40 dB)
CMRR >40 dB at VCM=+0.5, DC-10MHz

Testbench:



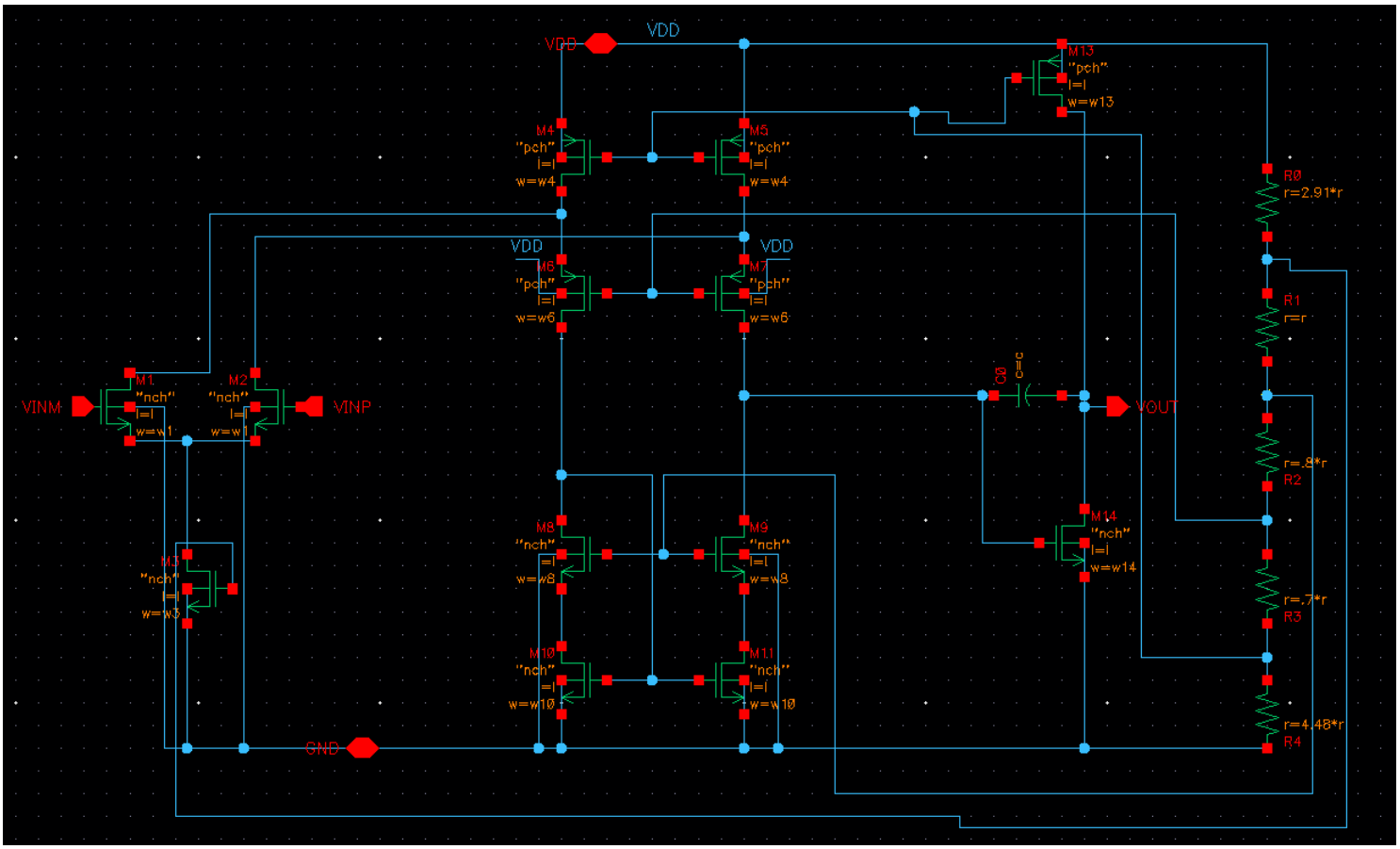
Results:



Red curve: ap = 0.5V, am = -0.5V, adc = 0V
Yellow curve: ap = 1V, am = 1V, adc = 0V

35.3279dB at 10MHz

Op-Amp Schematic: FC-CS design



Parameters:

	Name	Value
1	r	2.5K
2	c	1p
3	l	120n
4	w	160u
5	w1	w
6	w3	w
7	w4	.8*w
8	w6	.9*w
9	w8	.6*w
10	w10	.08*w
11	w13	.8*w
12	w14	w

All transistors are of the same length l=120n. Compensation capacitance of 1pF is used. Resistor divider is used from the power supply to bias. Width of transistors is variable as shown in the above table.
Biasing voltages are such that:
Gate of M3 is at Vnb1 = 703.2mV
Gates of M8 and M9 are at Vnb2 = 602.4mV
Gates of M6 and M7 are at Vpb2 = 521.8mV
Gates of M4 and M5 are at Vpb1 = 451.3mV

Table- SPICE performance vs Design objectives

Specification	SPICE performance
Maximum Settling Time: 8.0ns/8.0ns to within 0.5% of the output step size, settling up/settling down	Settling down: 6.942ns, Settling up: 6.113ns
DC Power Consumption measured with VIN=0.5 and (VOUT=0.5): 1.5mW.	1.41mW
Thermal Noise: < 300 uV rms, output referred. Integrate output noise from 1MHz to 500 MHz.	284.5u
DC Small Signal Differential Gain (measured open-loop): > 1,200	10336.5
Output Swing (measured open-loop without any load): Within 0.25 V of both VDD=1.0 and AGND=0. (Defined as max. output range for which the incremental gain vo/vid is still at least 500)	We see an output swing of 82.4929mV to 1V where gain>500. At 249.527mV, gain=5.28331k At 751.633mV, gain=7.9436k
Phase Margin 1pF load: At least 60deg at the feedback factor f=0.5	66.904 deg at gain-of-2 crossover frequency of 96.1127MHz.
PSRR+(from VDD) >40 dB at DC-10MHz	PMRR = 40dB till 1.4MHz 35.42469dB at 10MHz
CMRR >40 dB at VCM=+0.5, DC-10MHz	CMRR = 35.3279dB at 10MHz

Discussion:
Unfortunately, my op-amp falls short of CMRR and PSRR specifications by less than 5 dB. I think the PSRR falls short as 7 transistors (or 4 bias voltages) are directly controlled by the power supply through a resistor network which does little to mitigate the noise. The noise is hence reaching the output. Impedances at both the terminals are not perfectly matched (We also see an offset of about 0.36mV). This probably results in bad CMRR.
On the other hand, this opamp provides a much higher open loop gain than that asked in the specifications (about 10x more), with a 65deg+ phase margin at gain-of-2 frequency, which makes it very stable. The settling times are both less than 7ns, again better than the asked for 8ns. It has a great output swing with almost the entire output range (Vout>82.5mV) giving a gain >500. There is no ideal current source used, which would be difficult to make and the entire opamp works from just one power supply. (VCM is used just for input, not biasing).
Started design with the above parameters. Wasn’t able to meet specifications. Started changing biases and widths to first obtain correct gain and phase. Then, settling time and noise. Output swing automatically achieved.

Table- hand design vs SPICE parameters:

Parameter	Value: Hand design	Value: Final
w	160u	160u
l	120n	120n
w1, w2	w	w
w3	w	w
w4, w5	w	.8*w
w6, w7	w	.9*w
w8, w9	w	.6*w
w10, w11	w	.08*w
w13	w	.8*w
w14	w	w
c	1pF	1pF
Vnb1	.58V	.703V
Vnb2	.55V	.602V
Vpb1	.48V	.522V
Vpb2	.42V	.451V

Major changes: Vnb1 goes up by almost 0.12V than calculated. w10-11 are much lower, w8-w9 are half.
Rest same or similar to hand calculations with minor changes.

Hand design:

As done in pset 5, we generate g_m vs I_D, gain vs I_D, f_T vs I_D plots. The difference is we don't known what the unit gain frequency is, and we are free to choose what we want.

Let's have a gain-of-2 frequency of 100MHz.

(Here we want PM > 60deg. Don't care about stability at unit gain).

$f_T = 10 \times (2 \times 100M) = 2\,GHz$.

Input is at nmos this time. (unlike PSET 5)

$2\,GHz \rightarrow I_D \sim 555.366\,nA/\mu m$ for $L = 120nm$.

with a $g_m r_o = 185$.

folded cascode has a gain of $\sim (g_m r_o)^2 \rightarrow$ which is good. (keeping, higher as might drop later).

$g_m = 9\,\mu S$.

~~$C_c = 2C_{GM_1}$~~ ~~GM_2~~.

~~load cap 1pF~~ $C_2 = 1pF$.

$\frac{g_m}{C_c} = 200 \times 2 \times \pi \times 10^6$.

~~$C_c = 2C_{GM_1}$~~ we don't have anye R_2.

~~But we have $C_2 = 1pF$, $C_c \rightarrow 0.5pF$ / $1pF$?~~

$GM_2 = 2GM_1$

~~Slew Rate = $\frac{\min(I_1, I_2)}{C_2}$.~~

$$C_c = \frac{g_{m_1}}{\omega_{unity\text{-}gain}}.$$

Arbitrarily choosing $C_c = 1pF$.

$$2\pi \times 10^{-12} \times 200 \times 10^6 = g_{m_1} = 0.2mS \times 2\pi.$$

$$2\pi \times 0.2 \times 10^{-3} \times \frac{}{W} = 9 \times 10^{-6}.$$

$W = 140\mu m$. (for higher gain. $W = 160\mu m$.).

Slew Rate = $\frac{\min(I_1, I_2)}{C_2}$

In specification 1: step size = 0.2V.

step < slewrate $\times \tau$

where τ is settling time constant time

: our phase is $> 60°$ spec.

for 0.5% tolerance error in settling time.

$$\frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} = 0.005 \Rightarrow e^{-\zeta\omega_n t} = 0.005 \times 0.8$$

$\sqrt{1-\zeta^2} \to 0.6^2 \approx 0.8$.

$-\zeta\omega_n t_s = -5.52$

$t_s = 5.52\tau$, Time const.

$t_s = 8\,ns$ given.

$\tau = \frac{8}{5.52} = 1.45\,ns$.

$\therefore 0.2\,V < \text{slew rate} \times 1.45\,ns$.

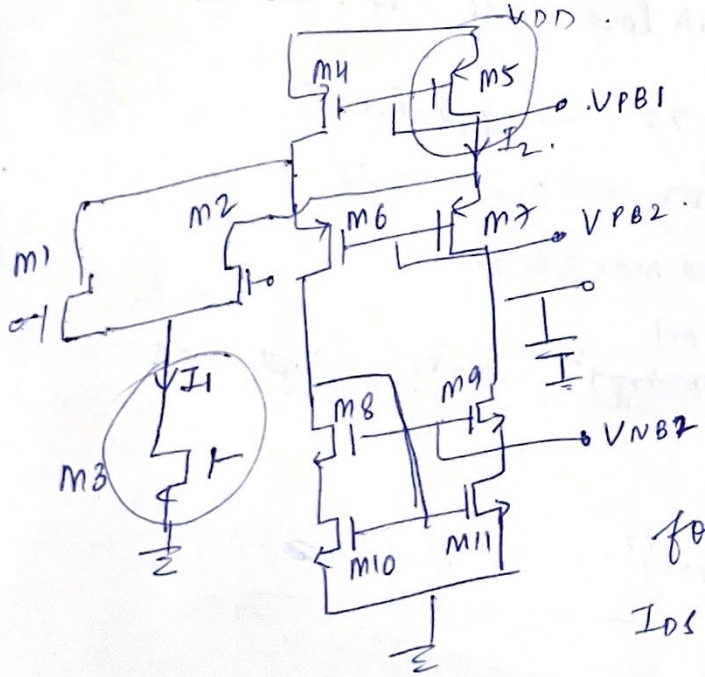
$1.38 \times 10^8 < \text{slew rate}$.

$C_2 = 1pF$, $C_C = 1pF$ (or 0.5?).

$\therefore \min(I_1, I_2) > 10^{-12} \times \underbrace{2}_{\text{additional in case cap higher.}} \times 1.38 \times 10^8$.

$\min(I_1, I_2) > 0.276\,mA$ or $276\,\mu A$.

~~[illegible] $\times$ [illegible] mA.~~



upon simulation.

PMOS $v_{th} \approx -370\,mV = 370\,mV$

NMOS $v_{th} \approx 510\,mV$

[range → have taken avg. as depends on other factors.

for M3.

$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(\frac{V_{GS} - V_{TH}}{2}\right)^2$

assuming saturation.

$$300\times10^{-6} = \frac{140\times10^{-6}}{120\times10^{-9}} \times \frac{(V_{GS}-0.52)^2}{2} \times 28.77\times10^{-3} \times$$

$$C_{ox} = \frac{8.854\times10^{-12}\times3.9}{1.2\times10^{-9}} \quad \text{SI units} = 28.77\ mF/m^2$$

Running 120n, 1u with $V_{GS}=0.6V$ ($V_{GS}>V_{TH}$), V_{DS} → 0 to 1V to obtain mobility in saturation.

~~$I_D = 28.7\times10^{-3} \times \frac{1u}{120\times10^{-9}} \times u\,(0.6-0.52)^2 \cdot (V_{DS}=0.3V)$~~

~~$3890\times10^{-6} = u$~~

V_{DS}

Better method is to just simulate nmos with $W=140u$, $L=120n$ and see what V_{GS} gives 300u.

$V_{GS} = 505mV \rightarrow 300\mu A$. $(V_{DS}=0.6V)$.

for PMOS.

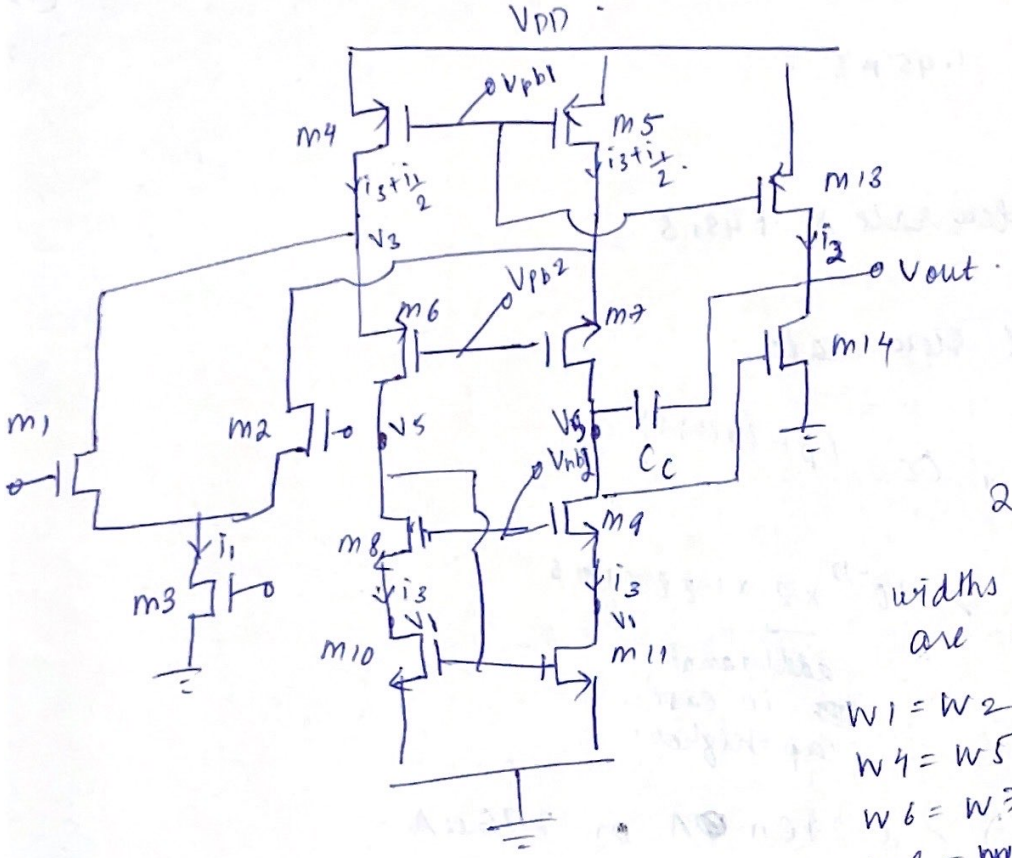
$V_{SG} = 470mV \rightarrow 300\mu A$. $(V_{SD}=0.6V)$.

Another way to look; we can assign current from power consumption spec.

Total current → 1.5mA.

1mA current mirror

0.5mA



(Note: there's no M12)

$i_1 = 0.5\,mA$ ⎫
$2i_3 + i_2 = 1\,mA$ ⎭ power spec

widths of these transistors are kept same.

$W1 = W2$
$W4 = W5$
$W6 = W7$
$W8 = W9$
$W10 = W11$.

All transistors are same length.

initially, all transistors are 'W'.

$V_{out} \rightarrow 0.25 - 0.75$ → specification.

let's design for $0.15 - 0.85$.

$V_{o,min} = 0.15$, $V_{o,max} = 0.85$.

$K_p = \mu_p C_{ox}$
$K_n = \mu_n C_{ox}$

$$2i_2 = K_p \frac{W_{13}}{L}\left(\frac{0.625 - V_{pb1}}{-V_{pb1} + V_{DD} - V_{t,p}}\right)^2 = K_n \frac{W_{14}}{L}\left(V_{out} - V_{tn}\right)^{0.52\ 2}$$

$W_{13} = 140\,\mu$

$$W_{13}(0.625 - V_{pb1})^2 = 3\,W_{14}(V_{out} - 0.52)^2$$

$V_5 - V_{thn} < V_1 \rightarrow$ M10, M11 sat.

$$2i_3 = k_n \frac{W_{10}}{L} (V_5 - V_{thn})^2$$

$V_5 > V_{nb2} - V_{thn} \rightarrow$ M8, M9 sat.
or. $V_{nb2} < V_{thn}$ → weak inv subthreshold.

$$2i_3 = k_n \frac{W_8}{L} (V_{nb2} - V_{thn})^2$$

or exp relation.

$I_0 e^{qV_{GS}/1.5KT}$.

$\therefore i_3 = I_0 e^{q(V_{nb2})/1.5KT}$.

$V_{thn} \sim 0.51V$
$V_{thp} \sim 0.37V$.
Pset 4-5.

for ease assume it's saturated.

$\therefore V_{nb2} > 0.51V$.

$V_5 + V_{thn} > V_{nb2} \rightarrow V_{nb2} < 0.66V$.

$\approx V_{out}$ (0.51)

$V_{out\,min} \rightarrow 0.15V$. → worst case.

$-0.51 < V_{nb2} < 0.66$.

$$2i_3 + \frac{i_1}{2} = k_p \frac{W_4}{L}\left(V_{DD} - V_{pb1} - V_{thp}\right)^2 \quad \text{— (1)}$$

M4, M5.

$V_{DD} - V_3 > V_{DD} - V_{pb1} - V_{thp}$.

$V_{pb1} + V_{thp} > V_3 \Rightarrow V_3 = V_{pb1} + V_{thp}$.

$$2i_3 = k_p \frac{W_6}{L}\left(V_3 - V_{pb2} - V_{thp}\right)^2$$

$$2i_3 = k_p \frac{W_6}{L}\left(V_{pb1} - V_{pb2}\right)^2 \quad \text{— (2)}$$

M6, M7.

~~$V_3 - V_5 > V_3 - V_{pb2} - V_{thp}$.~~

$V_{pb2} + V_{thp} > V_5$

power spec.

$0.5\,mA$

$$\left(V_{cm} - V_{thn}\right)^2$$

$0.5 \quad 0.52$

M1, M2.

$\therefore$ subthreshold.

from nmos id vs Vgs at $V_{DS} = 0.6V$.

$$2\left(\frac{i_1}{2}\right) = k_n \frac{W_3}{L}\left(V_{nb1} - V_{thn}\right)^2 \quad \text{— (3)}$$

$$1.63 \times 10^{-4} \times \frac{160 \times 10^{-6}}{120 \times 10^{-9}}\left(V_{nb1} - 0.51\right)^2 = 10^{-2}$$

$V_{nb1} = 0.58V$.

from pmos id vs Vgs.

$$2i_3 = 0.5\,mA + 1.78 \times 10^{-5} \times \frac{160\mu}{120n}\left(0.63 - V_{pb1}\right)^2 \quad \text{— (4)}$$

$$2i_3 = 1.78 \times 10^{-5} \times \frac{160\mu}{120n}\left(V_{pb1} - V_{pb2}\right)^2 \quad \text{— (5)}$$

$i_3 + \frac{i_1}{2} > 300\mu$ → from previous slew rate calculation. (→)

eqn 4 → $0.6\times10^{-12} = 1.78\times10^{-5} \times \frac{160\times10^{-6}}{120\times10^{-9}} (0.63 - V_{pb1})$

$V_{pb1} = 0.48V$

$\therefore i_3 + \frac{i_1}{2} = 300\mu A$ (for above value).

$i_3 = 50\mu A$.

$10^{-2} \cdot 100\times10^{-6} = 1.78\times10^{-5} \times \frac{160\times10^{-6}}{120\times10^{-9}} (0.48 - V_{pb2})^2$.

$V_{pb2} = 0.42V$.

$i_3 = \frac{k_n}{2}\frac{W_8}{L}(V_{nb2} - V_{thn})^2$] M8, M9.
$- V_1$

$V_5 - V_1 > V_{nb2} - V_1 - V_{thn}$.

$i_3 = \frac{k_n}{2}\frac{W_{10}}{L}(V_5 - V_{thn})^2$

$V_5 - V_{thn} > V_1$

Limiting condition.

Let $V_5 - V_{thn} = V_1$.

$$\therefore i_3 = \frac{k_n}{2}\frac{W_8}{L}\left(V_{nb2} - V_{thn} - V_5\right)^2$$

$$50\mu = i_3 = \frac{k_n}{2}\frac{W_{10}}{L}\left(V_5 - V_{thn}\right)^2$$

$$50\times10^{-6} = \frac{1.63\times10^{-4}}{2} \times \frac{160\times10^{-6}}{120\times10^{-9}}\left(V_5 - 0.51\right)^2$$

$$V_5 = 0.53\,V.$$

$$50\times10^{-6} = \frac{1.63\times10^{-4}}{2} \times \frac{160\times10^{-6}}{120\times10^{-9}}\left(V_{nb2} - 0.53\right)^2$$

$$V_{nb2} = 0.55\,V.$$

All transistors used are W. May have to change widths later.