Modeling of Time Dependent Dielectric Breakdown in NMOSFETs

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Purpose

- A percolation model for bulk traps in the oxide is built, and is validated using experimental results.
- The failure time statistics and other parameters obtained experimentally for various devices are explained, while including interface traps and also extending the model for a bilayer (IL+HK) stack.
- A new possible explanation for difference in time kinetics slope of SILC and TDDB bulk trap is also proposed.

Introduction

- The gate oxide accumulates traps, due to stress, which eventually form a percolation path and causes transistor failure (TDDB).
- TDDB is statistical in nature and shows Weibull distribution, whose slope (β), in general, reduces with EOT scaling.
- The percolation model links β varies empirically with oxide thickness (T_{OX}) as

  $\beta = n*T_{OX}/a0$

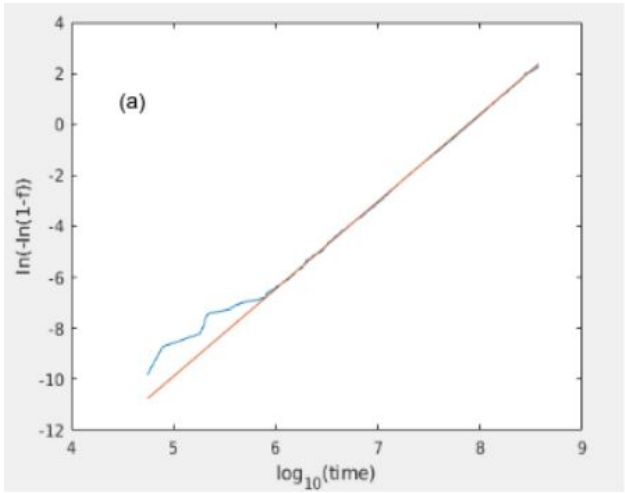
  where n is the time slope of bulk trap generation and a0 is the trap diameter.
- Weibull distribution in HKMG stacks shows dual slope: a higher one at low time to breakdown and reduces for higher time to breakdown.
- This can be explained by higher trap generation in the HK as compared to in IL.

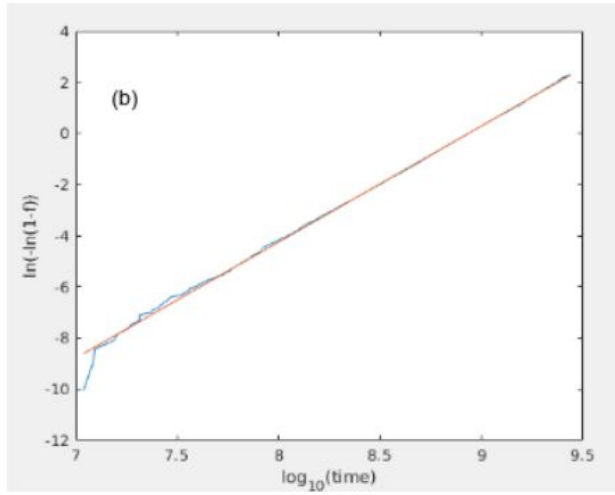
Past work

- Most reports on TDDB are focused on the voltage or oxide field (E_{OX}) dependence of bulk trap generation.
- Reports focusing on β vs T_{OX} variation show no concrete model with respect to n and a0 variation, or interface contribution consideration.
- There have also been doubts cast on the validity of SILC measurements as an experimental means to measure the density of defects generated.

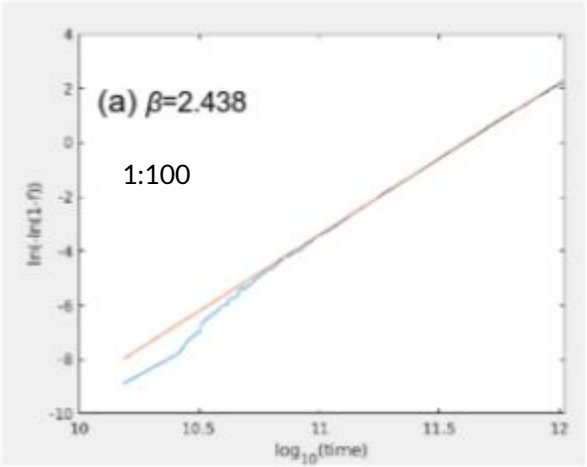
Work Done in Phase-I

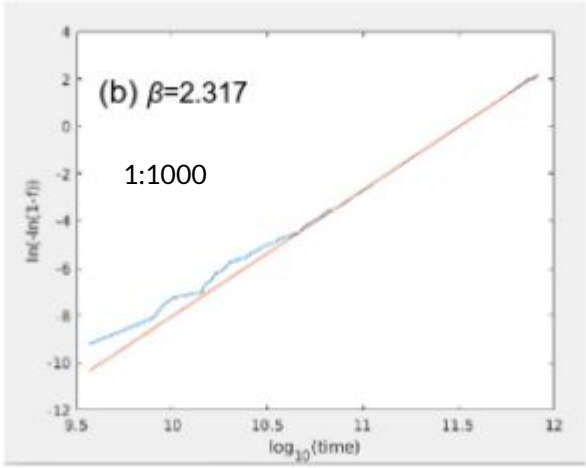
- **Percolation model is built and tested for various thicknesses and n.**
- **Interface traps integrated in the model and β variation shown.**

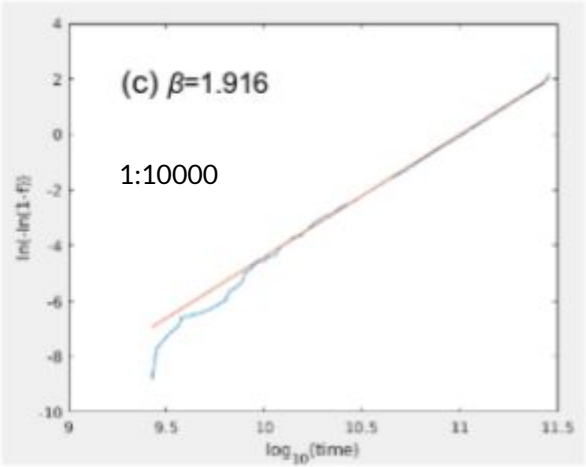




n=0.5, a0=0.5nm, A=0.5 (a) t_{OX} = 1.5nm, β = 1.49 (b) t_{OX} = 2nm, β = 1.97



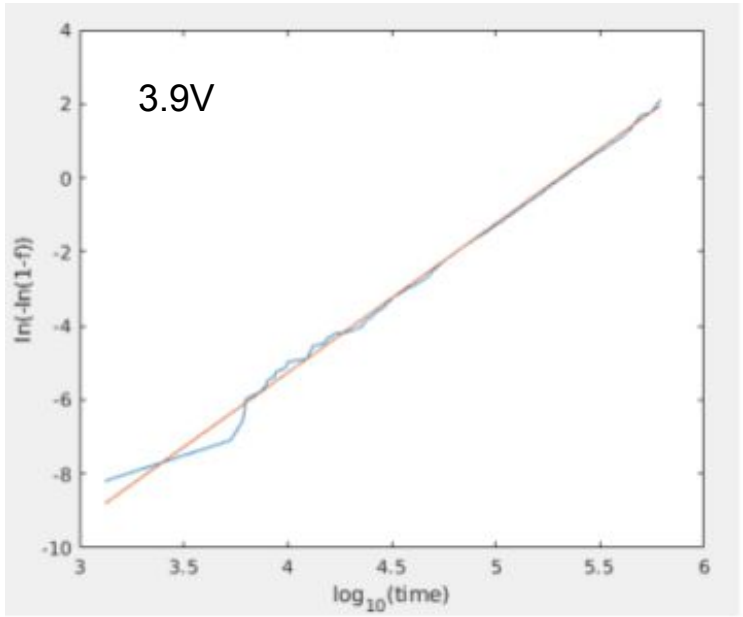


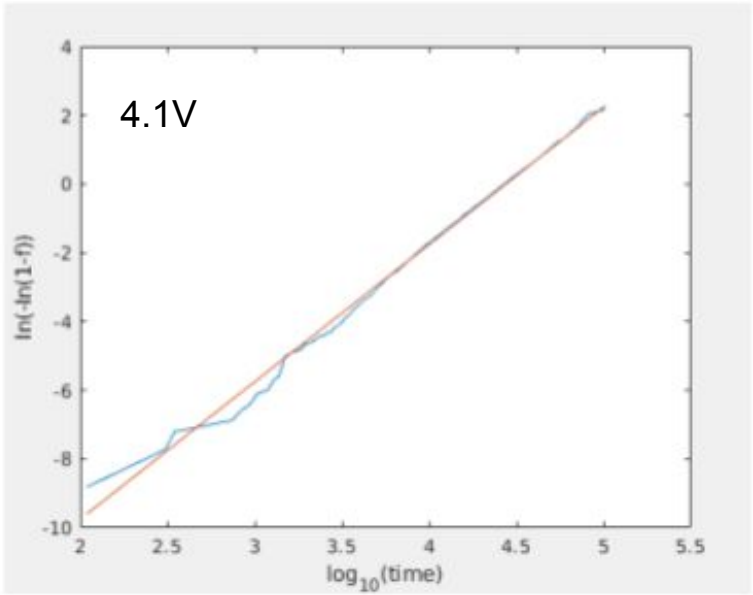


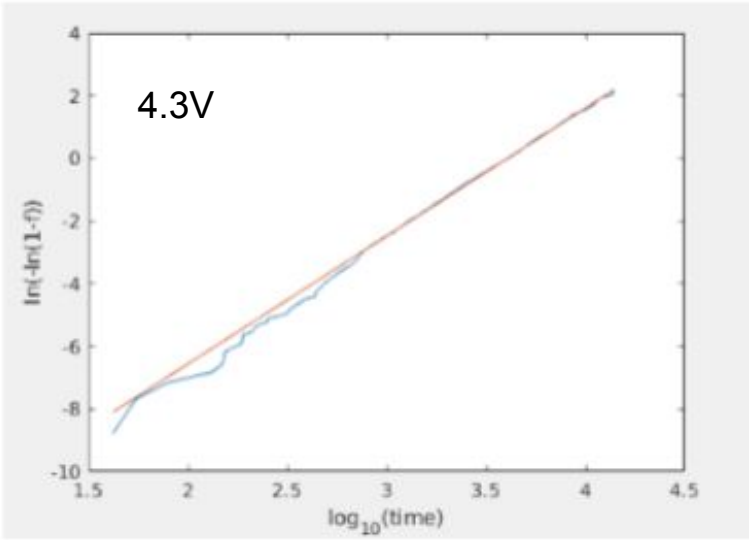
Work Done in Phase-II

- Experimental verification using data by Wu et al. and RDD modeling
- Data by Nicollian et al. to test the hypothesis of interface traps reducing β
- Modeling of β vs t_{OX} reported in literature
- Model to explain differences in SILC slope and bulk trap slope

Wu et al. Voltage Dependence







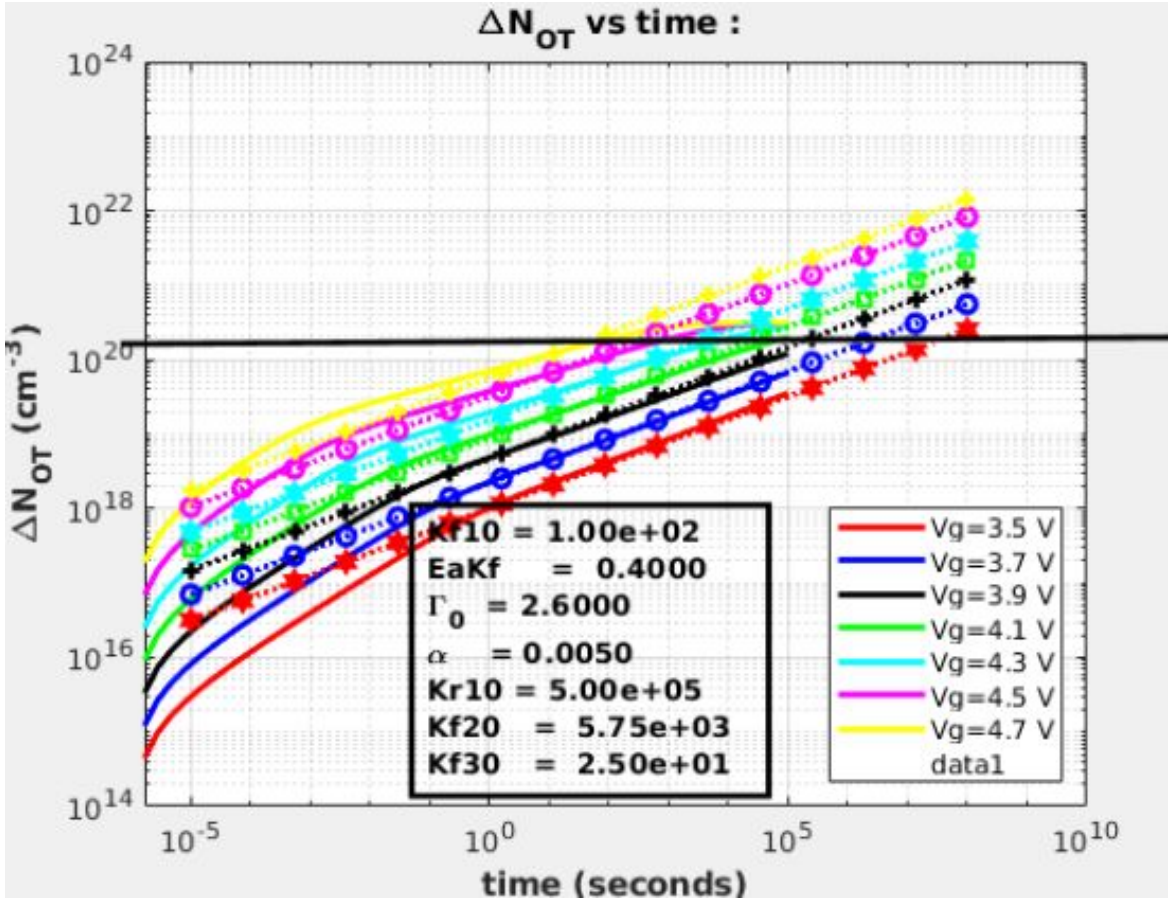
- **For β = 1.7, with t_{OX}=2.66 nm, n=0.3, a0=0.46 gives us 6 layers. We run for 3.5V-4.7V**
- **We verify the fixed time VAF of Wu et al., from our percolation too. (not shown here)**

[E. Y. Wu, et al. IEEE Transactions on Electron Devices, vol. 49, no. 12, pp. 2131–2140, 2002]

[E. Y. Wu, et al., IEEE Transactions on Electron Devices, vol. 49, no. 12, pp. 2141–2150, 2002]

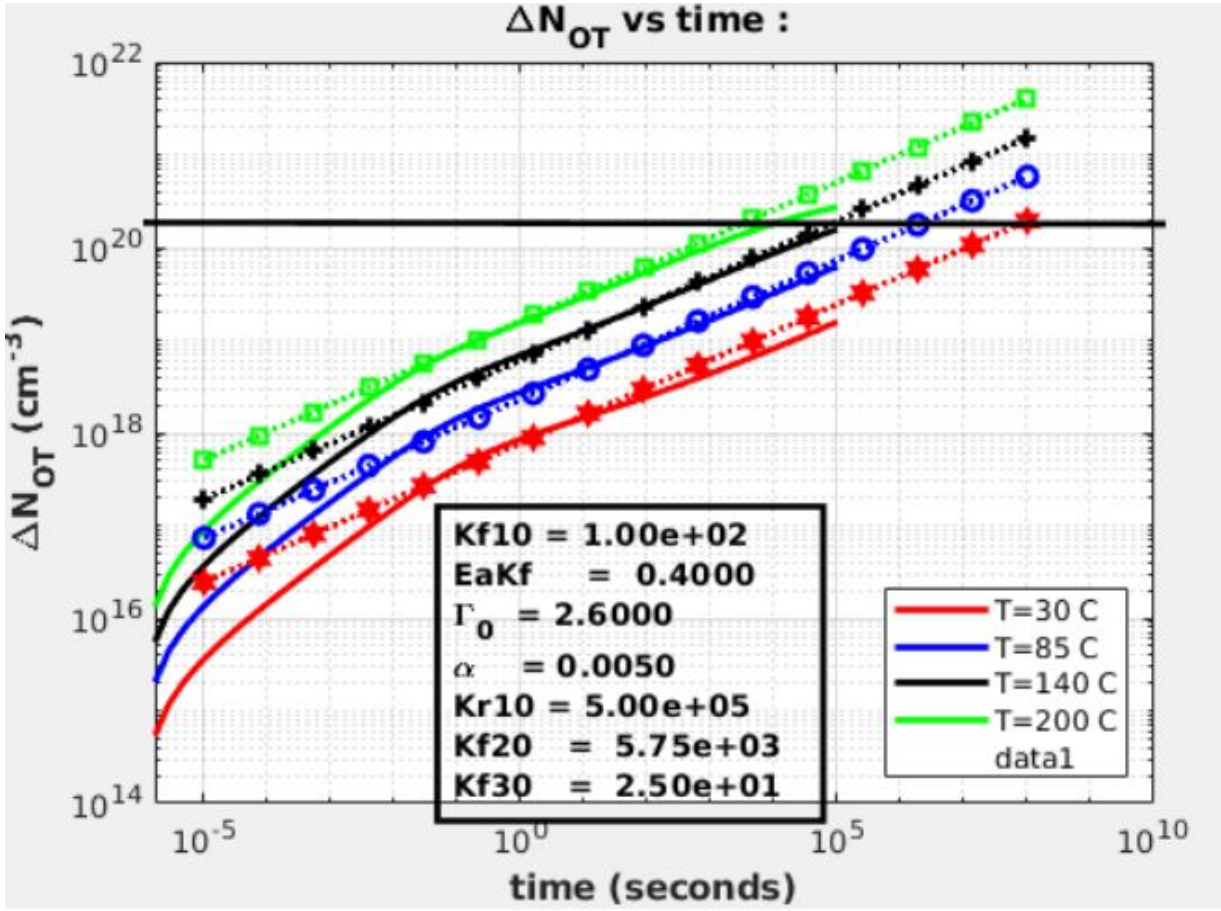
Wu et al. Voltage Dependence - RDD Modeling

- Using the percolation model, we obtain bulk trap time kinetics, and model it using RDD framework.
- The horizontal line is critical trap density to breakdown or N_{BD} (the trap density by which 63% of breakdowns).



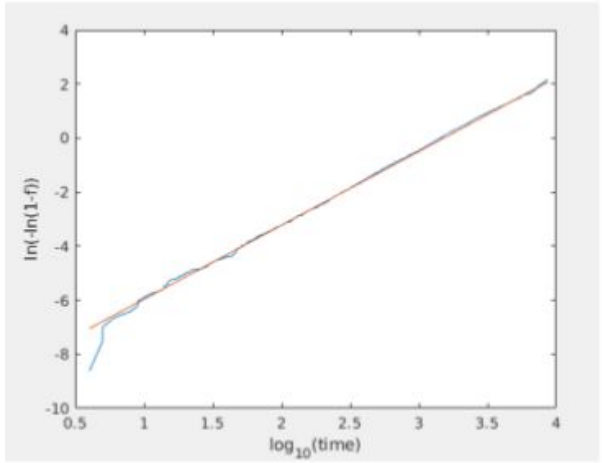
Wu et al. Temperature Dependence - RDD Modeling

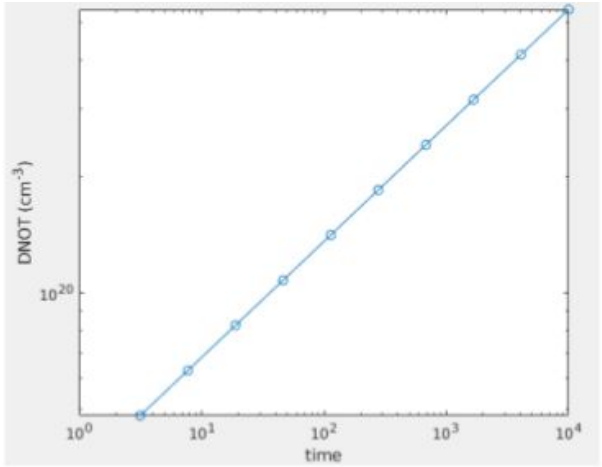
- We use percolation model for temperature modeling and verify activation energy.
- Bulk trap time kinetics for various temperature is obtained.
- Note that, same parameters as voltage modeling are used for temperature RDD modeling.

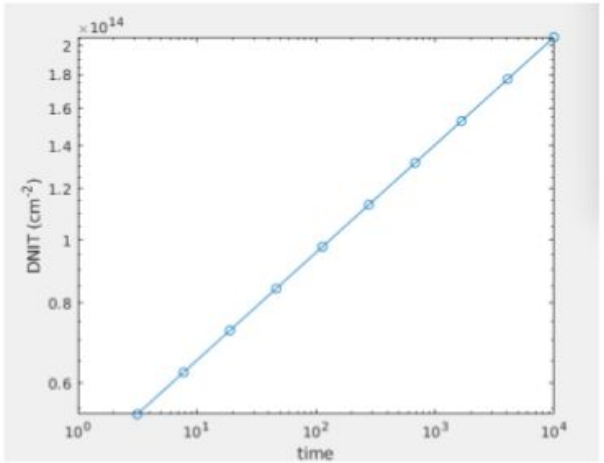


Nicollian et al.: β=1.17 keeping n=0.3 as Wu et al.

- There is still debate that to model β vs t_{OX}, n goes down or interface trap contribution comes in keeping the same bulk trap slope.
- Nicollian et al. have reported n =0.25. So, taking n =0.3, as in the case of Wu et al., we will add interface traps and see what interface trap density is required to pull the β down to what is reported by Nicollian et al.
- The TDDB percolation simulation at 2.3V with 1:10 bulk trap to interface ratio, the bulk trap density, the interface trap density are shown to obtain β=1.18.
- The the interface trap density is much higher than that reported in literature.



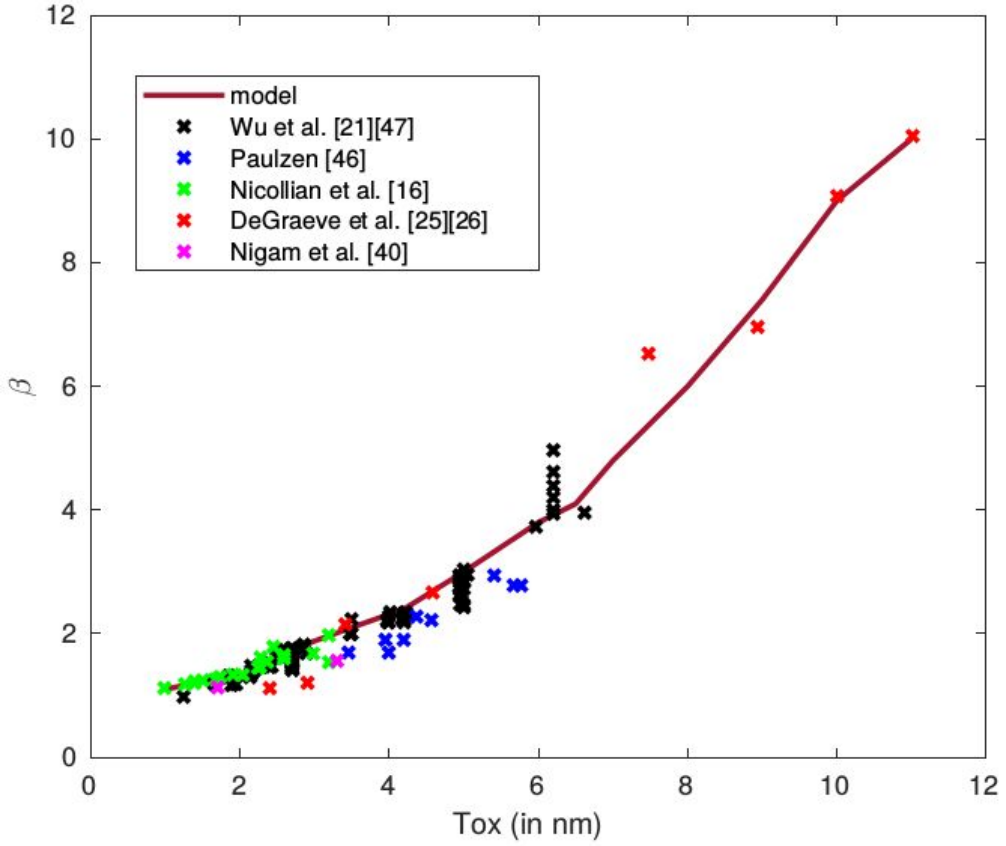


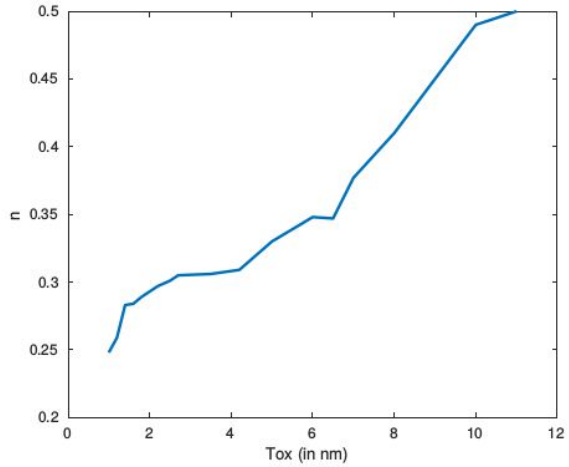


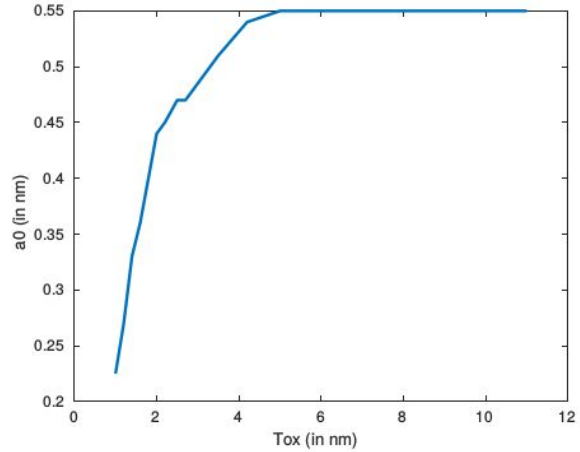
[P. E. Nicollian,et al. in IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE, 2005, pp. 392–395.]

β vs t_{OX} reported in literature and our model

We vary n and a0 as shown in a monotonic fashion and try to model using $\beta = n*T_{OX}/a0$

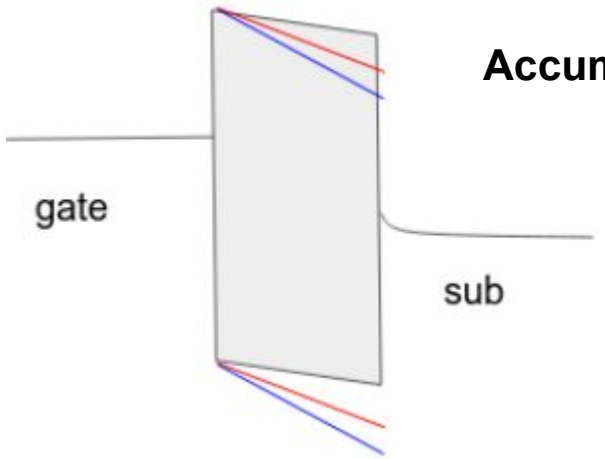


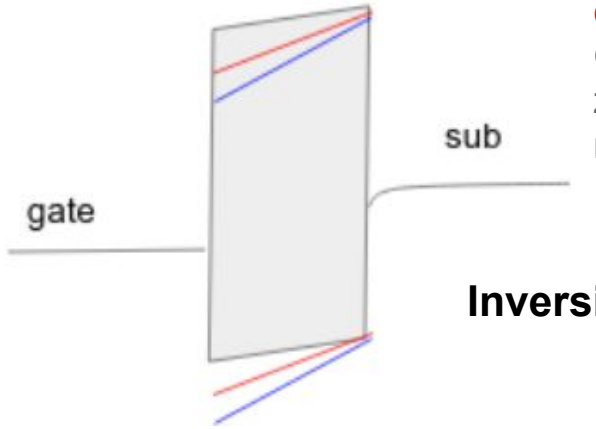




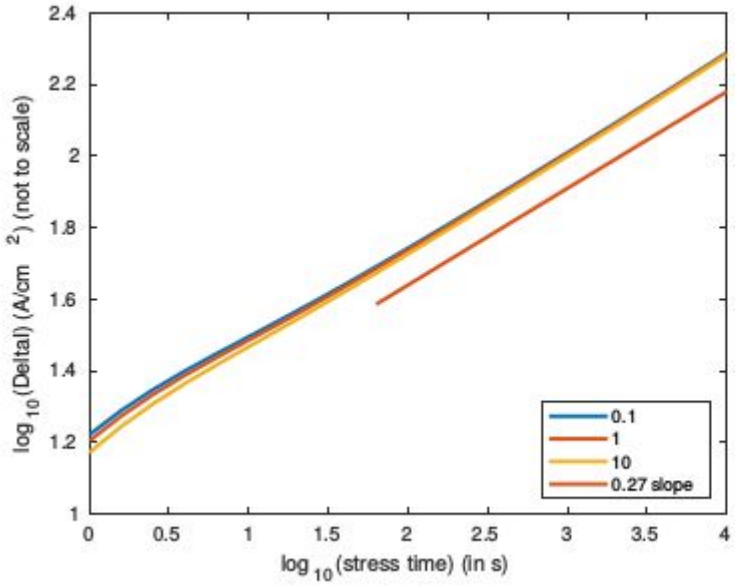
Differences in SILC slope and bulk trap slope

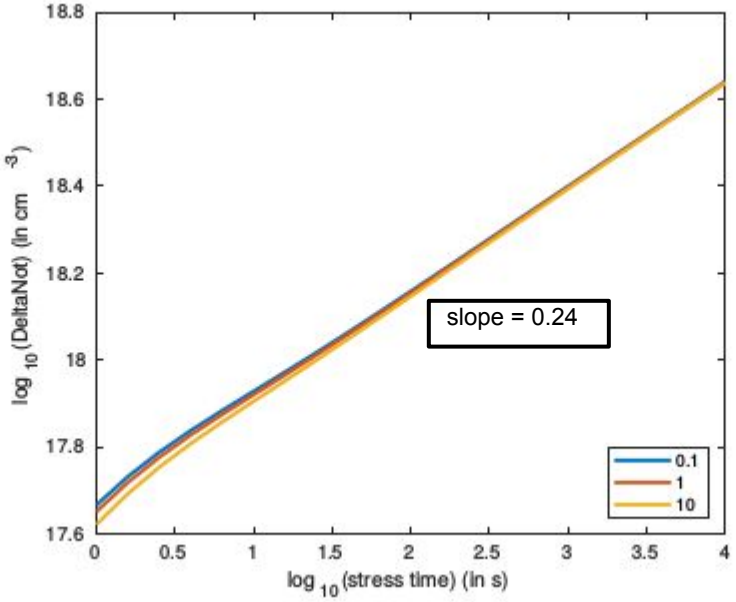
- **With the previous modeling, we see that n required for the bulk trap time kinetics is lesser than the reported SILC slope for a particular thickness.**
- **However, in our model we haven't considered the traps at the oxide-substrate interface which trap charges during stress.**
- **This is because as the stress time increases, the trapped charges increase, which result in more band bending, resulting in smaller barriers for TAT.**

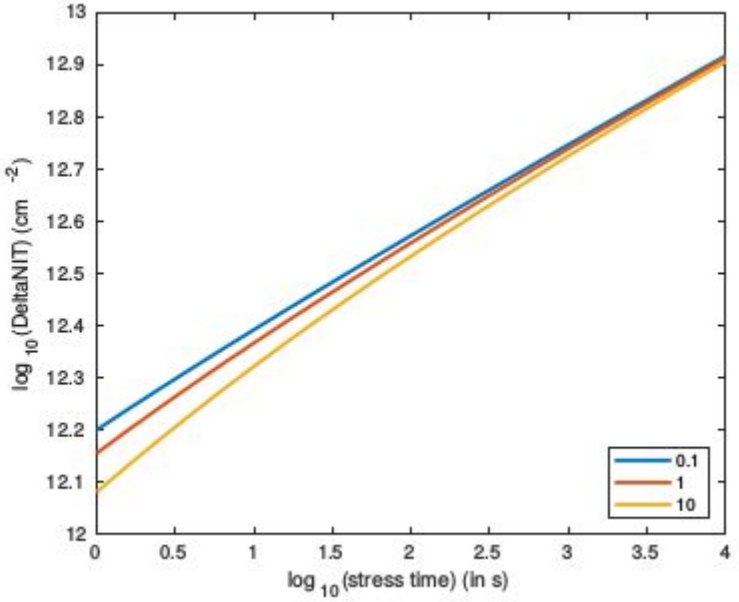




Blue: at stress voltage with charges trapped
Red: measurement voltage, but just after stress, more band bending due to additional charge in substrate as compared to grey
Grey: measurement voltage, zero charge (long time after measurement, all recovered).

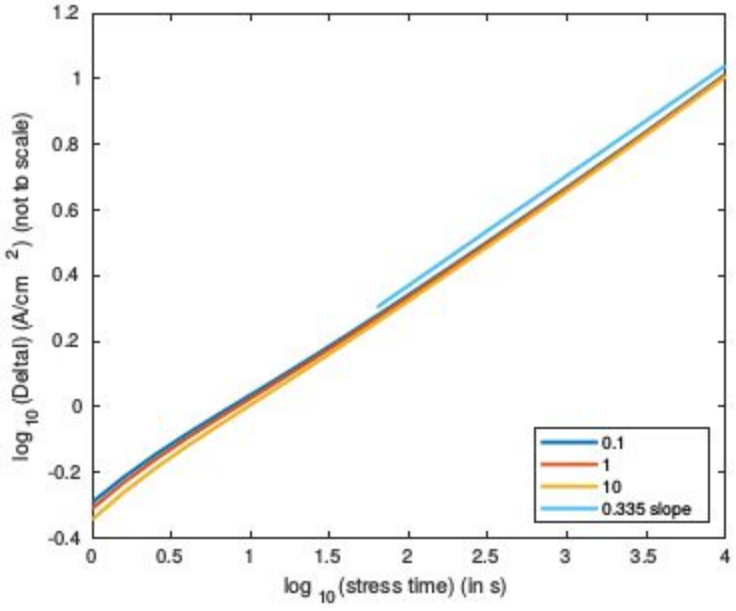


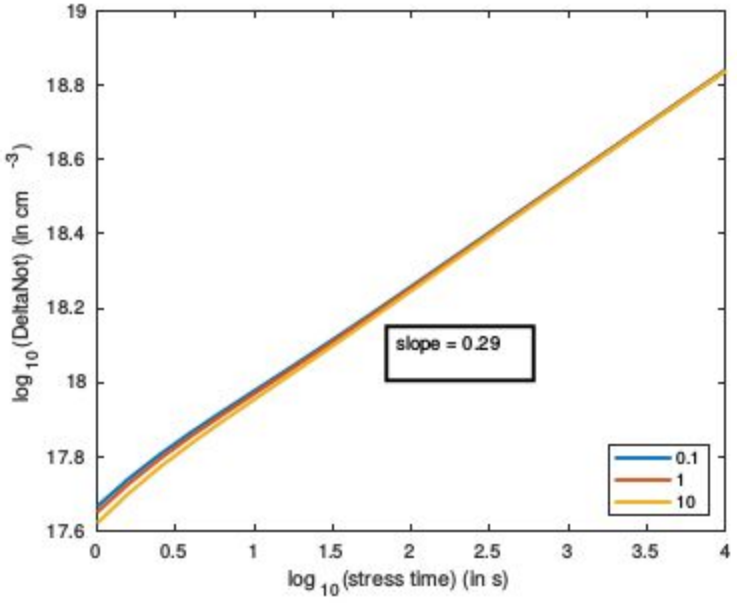


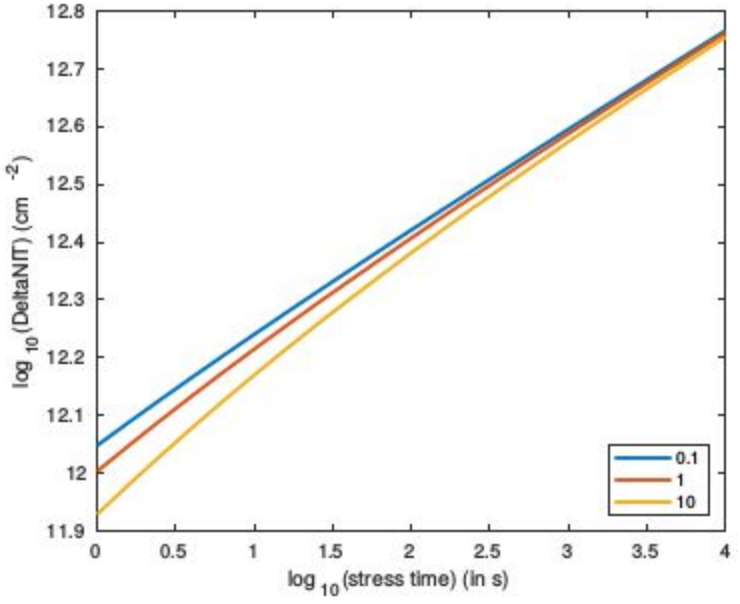


Keeping a bulk trap slope of 0.24 according to our model for 1.2 nm, we obtain a SILC slope of 0.27

[P. E. Nicollian, et al. in IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE, 2005, pp. 392–395.]

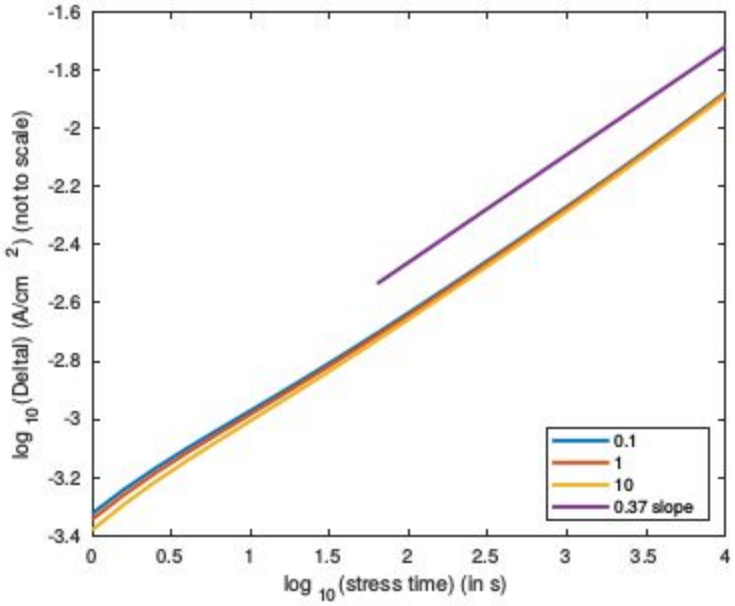


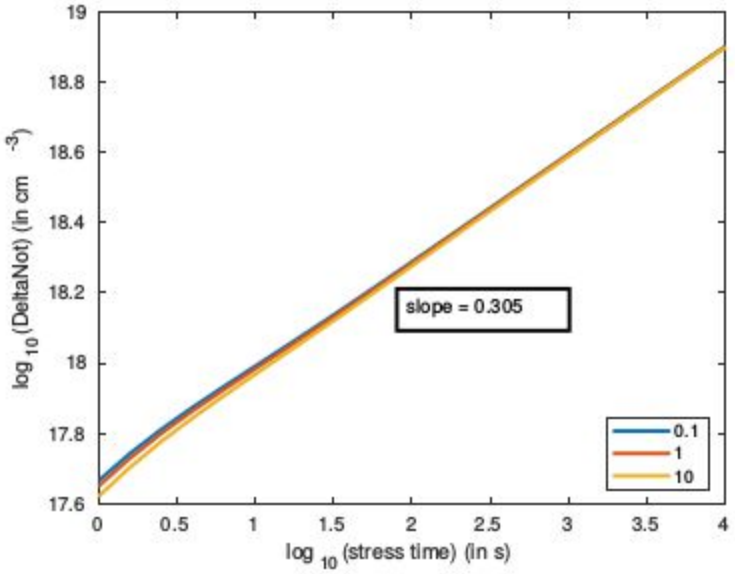


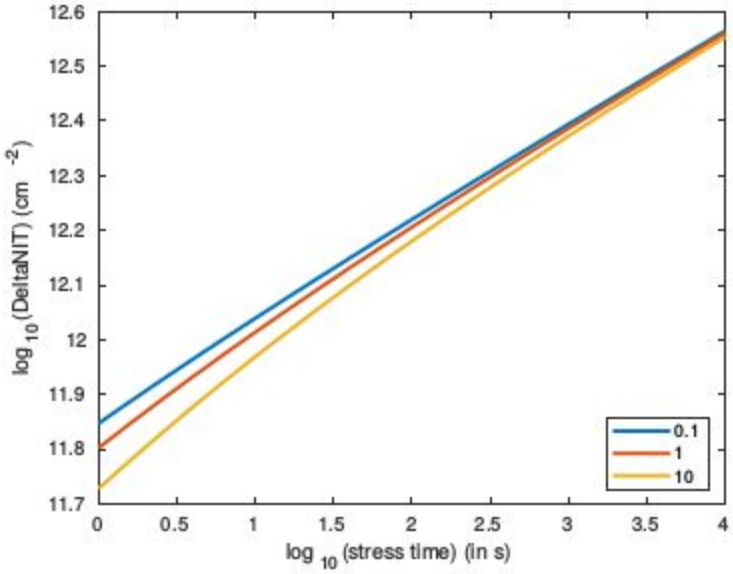


Keeping a bulk trap slope of 0.29 according to our model for 1.7 nm, we obtain a SILC slope of 0.335. Reference reports SILC slopes in the range of 0.3-0.35

[T. Nigam, et al., in 1999 IEEE International Reliability Physics Symposium Proceedings. 37th Annual (Cat. No. 99CH36296). IEEE, 1999, pp. 381–388.]

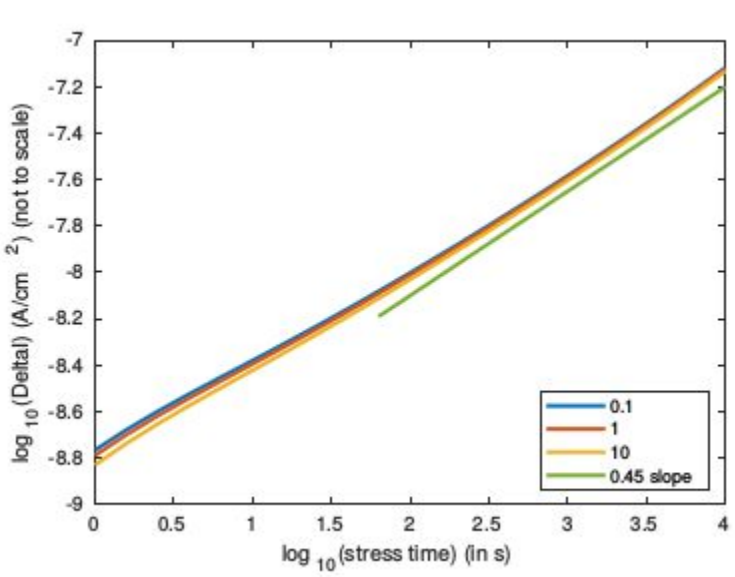


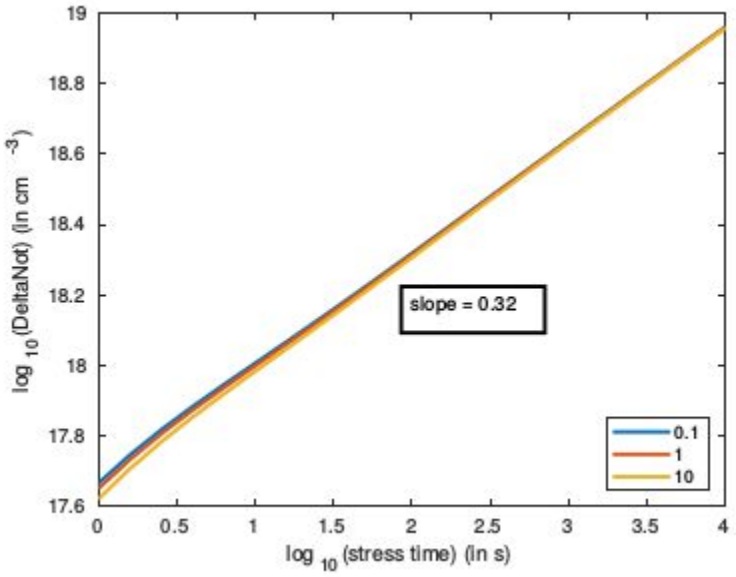


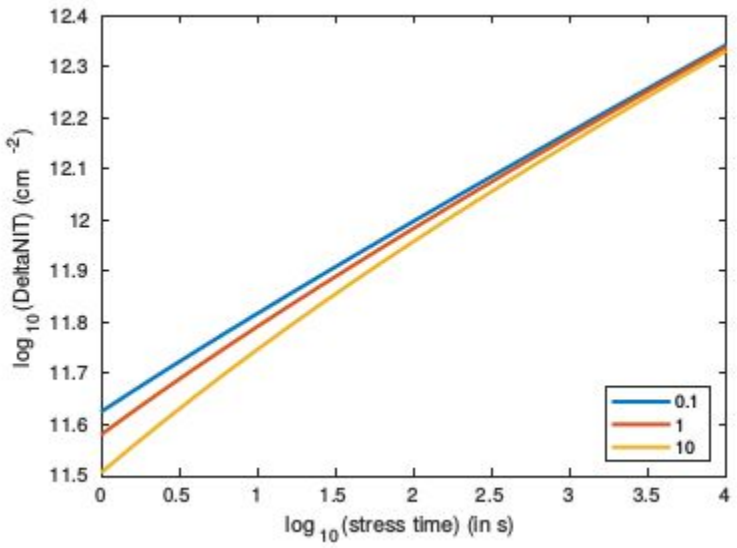


Keeping a bulk trap slope of 0.305 according to our model for 2.7 nm, we obtain a SILC slope of 0.37. Reference reports SILC slope as 0.36.

[E. Y. Wu, et al., IEEE Transactions on Electron Devices, vol. 49, no. 12, pp. 2141–2150, 2002]







Keeping a bulk trap slope of 0.32 according to our model for 4.5 nm, we obtain a SILC slope of 0.45. Reference reports SILC slope as 0.5

[K. Okada, et al. in 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216). IEEE, 1998, pp. 158–159.]

Summary

- Percolation model for TDDB is built and experimental results verified. Changes in β due to n and a0 variation are shown.
- Interface traps are probably not the full reason for β reduction is shown.
- A new model for explaining the differences in SILC and bulk trap slopes is presented.